The *Star-10*© Transceiver

In Part 1 of this series, we learn about some of the design criteria involved in high performance, fully synthesized, continuous coverage, coherent transceivers.

Cornell Drentea, KW7CD

Introduction

It has always been the dream of the technically inclined radio amateur to build his or her own equipment from scratch. Such has been the case in the first part of the 20th century, when Amateur Radio equipment was relatively easy to construct, allowing for simple home building. While single-band or band-switched equipment has been relatively easy to realize, RF design has recently evolved into a complex art of mixed technologies using new solid-state components, novel frequency generation techniques, microprocessors, digital logic and signal processing techniques that have exceeded the capabilities of the average amateur operator. This, in turn, has put the design of complex high performance radio equipment beyond the scope of the casual experimenter or equipment builder, forcing hams, more and more, to become appliance operators. Increasingly sophisticated equipment design has presented a steep learning curve even for the most capable home builder or the modern radio equipment manufacturer.

In the past, many construction articles have been published regarding simple radio projects. Dedicated single-band or limited band-switched, down-conversion superheterodyne receivers and transceivers have been published extensively in the literature. More recently, so-called "software defined radios," using old-fashioned zero IF direct conversions combined with new personal computer digital audio cards have evolved. Their performance has been controversial, only to be obscured by their perceived "flexibility."

Less published have been multi-band radios, due to their increased band switching complexity. Even less attempted have been full coverage high performance professional grade, up conversion / down conversion transceivers featuring fully synthesized, high resolution, coherent schemes used in conjunction with front-end automatically switched half-octave filter banks to ensure consistent high dynamic range performance over several octaves. Such designs have been left to the professional manufacturers, who can invest significant amounts of money and engineering resources over long periods of time for gain and profit.

This situation need not be so. With enough dedication, today's technically inclined ham is fully capable of developing full coverage, high performance transceivers that can compete in performance and features with their professional counterparts, and even outperform these designs.

This series of articles describes the development of just such a transceiver, the *Star-10,* a high dynamic range, fully synthesized coherent RF system that tunes continuously from 1.8 MHz to 30 MHz using microwave synthesis, coupled with true automatically switched (using miniature RF relays) half-octave filter banks, using a 10 Hz ultimate step resolution. This work is intended to inspire the radio amateur and the professional engineer alike, regarding modern, full coverage transceiver design.

The *Star-10* transceiver bears its name in good memory of an ambitious project I had been associated with in my youth — a product

The completed *Star-10* transceiver is designed to receive and transmit anywhere from 1.8 MHz to 30 MHz with a resolution of 10 Hz. It provides full cross mode, end-to-end RX/TX Split operation with a transmitter RF power of 100 W (125 W peak). The receiver has a composite spurious-free linear dynamic range in excess of 150 dB. It exhibits an MDS of –136 dBm (absolute), a third-order intercept point of +45 dBm. A coherent DDS-Driven PLL microwave synthesizer provides close in phase noise performance of –133 dBc/Hz. Receive spurious image rejection is –75 dB and transmit harmonic rejection exceeds –55 dBc. The transceiver uses a coherent up-convert down-convert superheterodyne approach.

The electrical and mechanical design features a modular approach using eighteen double sided, plated through printed circuit boards housed in machined, irradiated aluminum assemblies, all packaged in a custom made, hammer-tone finished cabinet measuring 15.5 x 6 x 11 inches.

757 N Carribean Ave
Tucson, AZ 85748
cdrentea@aol.com

that has never happened. It is the culmination of several years of RF design and development and reflects a state-of-the-art approach to HF transceiver design. The implementation encompasses the many phases of engineering and development usually encountered in a complex commercial or military piece of equipment, from the system design through the circuit and software design, the multiple brass boarding, the complex testing, and packaging into a final form factor as shown above.

The *Star-10* transceiver was designed to receive and transmit seamlessly with an ultimate tuning resolution of 10 Hz anywhere in its four-octave frequency range, covering any HF ham band, past, present and future, and featuring high dynamic range performance exceeding even today's most modern professional transceivers. Its receiver features a composite spurious free linear dynamic range exceeding 150 dB over the entire frequency coverage. In addition, this transceiver is capable of transmitting in several modes, 100 W of RF (125 W peak) power from 1.8 to 30 MHz. Transmitter harmonic rejection and receiver image rejection meet or exceed commercial equipment requirements. (See the Specification section of the text.)

The transceiver's entire capability is slaved to a powerful 8 bit PIC microprocessor that runs approximately 10,000 lines of code continuously at 32 MHz (above the HF range to keep spurious products out of the receiver's input range) in a closed loop, only to be interrupted by its keypad or RS-232 commands. The *Star-10* has been designed with a flexible and friendly human interface that can only be compared with the feel of classic HP test equipment.

The Challenge

The *Star-10* project first evolved in the 1980s (see References 1 and 2) and has been recently upgraded using the previously designed half octave filter banks as combined with the latest state-of-the-art microprocessor, DDS-PLL and high dynamic range RF technologies. As such, the command and control system of the old *Star-10* design (see References 1 and 2) has been physically reduced from its old hardwired static logic implementation of over thirty integrated circuits, to a simple command and control board containing a single microprocessor and a minimum of additional control circuits. The complexity of the entire command and control functionality of the transceiver has been moved into software containing approximately 10,000 lines of code. See Figure 1.

Although the hardware command and control section was simplified from the previous design, the new design has a new front end, a new first IF, a new logarithmic/linear second IF, specially designed crystal filters, and a new microwave synthesizer (see References 3 and 4), which all have contributed to increased dynamic range. This will be described in detail later. In the interest of making this article series as short as possible, and because of the complexity of this project, block diagrams, simplified schematics and test specifications are used throughout the article. Consequently, there are no boards, parts or software available from this source.

The *Star-10* transceiver has been a unique research experience into understanding what can be done — from the point of view of the laws of physics — in receiver and transceiver dynamic range performance. This research has been performed over a period of five years with parts, technologies and packaging means available to me at the time. The transceiver has been implemented with some unique parts that may not be available anymore. The *Star-10* development has been a purely scientific endeavor, intended primarily to understand what could be done to achieve ultimate receiver performance. Although the results have been outstanding, slightly better results may be possible using newer technologies and parts. The *Star-10* project was not intended as a commercial product. Its duplication is not economically feasible.

Acknowledgements

This project has been an ambitious scientific undertaking, developed with a considerable investment, equivalent to the price of a top of the line transceiver and with additional help. Because of the complexity of this transceiver, there are no circuit boards or software available.

Many thanks are extended to several individuals and companies who made contributions toward this development. Special thanks go to Chris Sisemore, who took my complex system mathematics and developed approximately 10,000 lines of perfect code for the command and control section of the transceiver. His technical discipline and diligent work with me in testing the brassboards of the system over a period of better than a year in the command and control section of the transceiver have paid off in achieving a flawless system performance and a most friendly operator interface.

Additional thanks go to Randy Burcham, KD7KEQ, who laid out (sometimes twice) the complex double sided, plated through printed circuit boards. His special attention to multiple stitching of ground planes and to properly placing the RF components have made for well-behaved high gain amplifier circuits that did not oscillate, and quiet synthesizer circuits. He also fully documented the entire design in a true engineering fashion using D-size engineering drawings.

Equal thanks go to Constantin Popescu, KG6NK, who worked diligently with me, breadboarding and testing the system before layout in his well-equipped laboratory. He has also been very instrumental in the harnessing and troubleshooting of the final system implementation. Additional thanks go to George Cutsogeorge, W2VJN, of In-

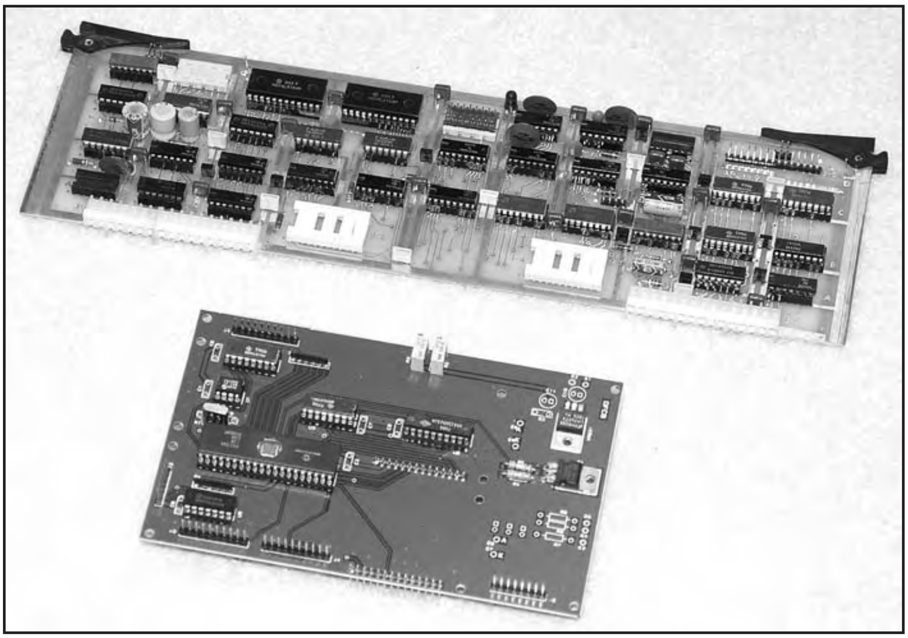


Figure 1 — The original *Star-10* command and control board (top) contained over thirty ICs. It has been replaced in the new design (bottom) by a single microprocessor controller chip and a minimum of additional circuits. Approximately 10,000 lines of software code have replaced the original hardwired logic functionality of the 1982 circuitry (See References 1 and 2).

ternational Filter Company who developed the high performance ultimate bandwidth IF crystal filters, Jerry Buckwalter of Alpha Components company, who developed the demanding high-intercept fundamental-type first IF roofing filters, the TEMEX Corporation who developed additional roofing filters, Ulrich Rohde, N1UL, of Synergy Microwave, who donated a low noise microwave VCO for the frequency reference unit (FRU) synthesizer and reviewed this article series, as well as to Peter Chadwick, G3RZP, of the former Plessey Company who donated samples of the high performance professional grade aerospace PLL chip used in the FRU. Additional thanks go to the Alinco Corporation, who made power transistors and other parts available for the power linear amplifier.

Finally, many thanks go to Phil Aide, KF6ZZ, who applied his switching power supply aerospace experience to develop a

Specifications

General

- Frequency coverage
  - RX: 1.8 MHz to 29.99999 MHz in one band, continuous in 10 Hz
  - TX: 1.8 MHz to 29.99999 MHz in one band, continuous in 10 Hz
  - Split operation from 1.8 MHz to 29.99999 MHz, any mode (or cross mode)
  - Display: Composite 4 × 16 character, large green 320 × 240 dots LCD Twist Dot Matrix with green backlighting
- RX/TX Front end Filter system: Automatically switched independent half octave band-pass (RX) and high power low-pass (TX) filter banks:
  - 1.8 MHz to 3 MHz
  - 3 MHz to 4 MHz
  - 4 MHz to 6 MHz
  - 6 MHz to 8 MHz
  - 8 MHz to 12 MHz
  - 12 MHz to 16 MHz
  - 16 MHz to 24 MHz
  - 24 MHz to 30 MHz
- Modes: USB, wide, narrow; LSB, wide, narrow; CW, wide, narrow; RTTY/AFSK, PSK31, wide, narrow
- IF passband tuning (PBT): ± 1.5 kHz, all modes, RX and TX
- Receiver incremental tuning (RIT): ± 9.9 kHz
- Architecture: Coherent double conversion superheterodyne, first IF = 75 MHz, second IF = 9 MHz
- Roofing filter (75 MHz): 8 pole crystal filters in two banks, BW = 10 kHz
- Second IF (9 MHz) ultimate bandwidths: 32 pole cascaded, SSB 2.4 kHz, 1.8 kHz; CW, RTTY/AFSK, 0.5 kHz; crystal filter insertion loss compensated automatically
- Second IF (9 MHz) gain = logarithmic linear 100 dB with 2.4 kHz crystal filter output for noise reduction using Analog Devices AD603 amplifiers
- Total AGC range: 80 dB nominal, 120 dB total (AIPA + BIPA + 9 MHz AGC)
- AGC attack time <2 ms, Decay time 4 seconds (SSB), 1 second (CW)
- System warm-up time to 1×10^{-8} <30 seconds
- Tuning speed: <10 ms
- S-meter: Calibrated in dBm and S units (within 2 dB)
- Digital memory channels: 99 (2 scan edges)
- RF output power (continuously adjustable):
  - SSB/CW/AFSK/RTTY: 0 to 100 W (125 W peak)
- Modulation:
  - SSB/RTTY/AFSK: Class III — High level double balanced modulator used
  - KCW: Class III — High level double balanced modulator carrier insert
- Spurious emissions: Equal or better than –55 dBc
- Carrier suppression: Equal or better than –65 dBc
- Unwanted sideband suppression (16 pole filters used): Equal or better than –65 dB
- Phase noise RX/TX: –133 dBc/Hz close in
- Spurious RX/TX: –75 dBc or better
- RX sensitivity (500 Hz ultimate bandwidth): –136 dBm (absolute) with 32 pole filters cascaded (plus 8 pole roofing filter)
- RX IIP3: +45 dBm
- RX composite linear DR: Equal or better than 150 dB (500 Hz, Preamp on, all AGCs on)
- RX IP3SFDR: At least 130 dB (20 kHz tone spacing) (500 Hz, preamp on, all AGCs on)
- RX blocking dynamic range: Will receive a –110 dBm signal with 25 dB SNR in the presence of a –20 dBm signal located 5 kHz away (500 Hz ultimate BW, preamp on, no attenuators, no AGC action)
  - Advanced intercept point attenuator (AIPA): Programmable –3 dB, –6 dB, –10 dB steps
  - Preamplifier Gain: +10 dB
  - RF/IF gain PIN attenuator (BIPA): 30 dB front panel adjustable
- RX noise figure at MDS: 15 dB (no AGC action)
- Selectivity:
  - SSB — USB, LSB selectable: 2.4 kHz, 1.8 kHz, at –3 dB cascadable from 16 poles to 24 poles
  - CW, RTTY/AFSK/PSK31, USB, LSB selectable: 1.8 kHz and 500 Hz/–3 dB: composite cascadable to 32 poles (plus 8 pole roofing filter)
- Image and spurious rejection: Equal to or better than –75 dB
- AF output power: 2.6 W at 10% distortion with an 8 Ω load
- Spectrum analyzer output (75 MHz or 9 MHz ± 250 kHz)

Synthesizer — Frequency Reference Unit (FRU)

- DDS Driven PLL 0.75 to 1.05 GHz divided by 10, for 20 log 10 (20 dB) phase noise improvement
- FRU frequency resolution: 10 Hz (1 Hz at DDS frequencies)
- FRU phase noise RX/TX: –133 dBc/Hz close in
- FRU spurious rejection –90 dBc
- Tuning lock up time: continuous within <10 ms.

Master Reference Unit (MRU)

- 84 MHz — Phase locked to 10 MHz OCXO/WWV
- Aging 10 Hz in 20 years.
- Long term frequency stability over temperature: 1×10^{-8} provided by the 84 MHz master reference unit (MRU) — PLXO phase locked to a 10 MHz OCXO/WWV controlled on power up.
- MRU warm-up time to 1×10^{-8} < = 30 seconds from power up (system warm-up)
- MRU phase noise: –165 dBc /Hz close in or better

Power Supply

- Power supply in: 70 to 140 V ac, 50/60 Hz
- Power supply out (RX): 24.7 V dc at 2 A continuous, 3.5 A peak
- Power supply out 2 (TX): 13.7 V dc at 20 A max continuous
- Power supply spurious as seen by the receiver: –145 dBm at any frequency in the coverage or TBD
- Power consumption:
  - TX max dc power: 800 VA
  - RX standby dc power: 200 VA (typical)

Mechanical

- Dimensions (projections not included): 15.5(L) × 11(W) × 6(H) inches
- Weight: 30 lbs
- Antenna connectors: SO-239 (50 Ω) and BNC (50 Ω)
- Operating Temperature range: 0°C to +50°C

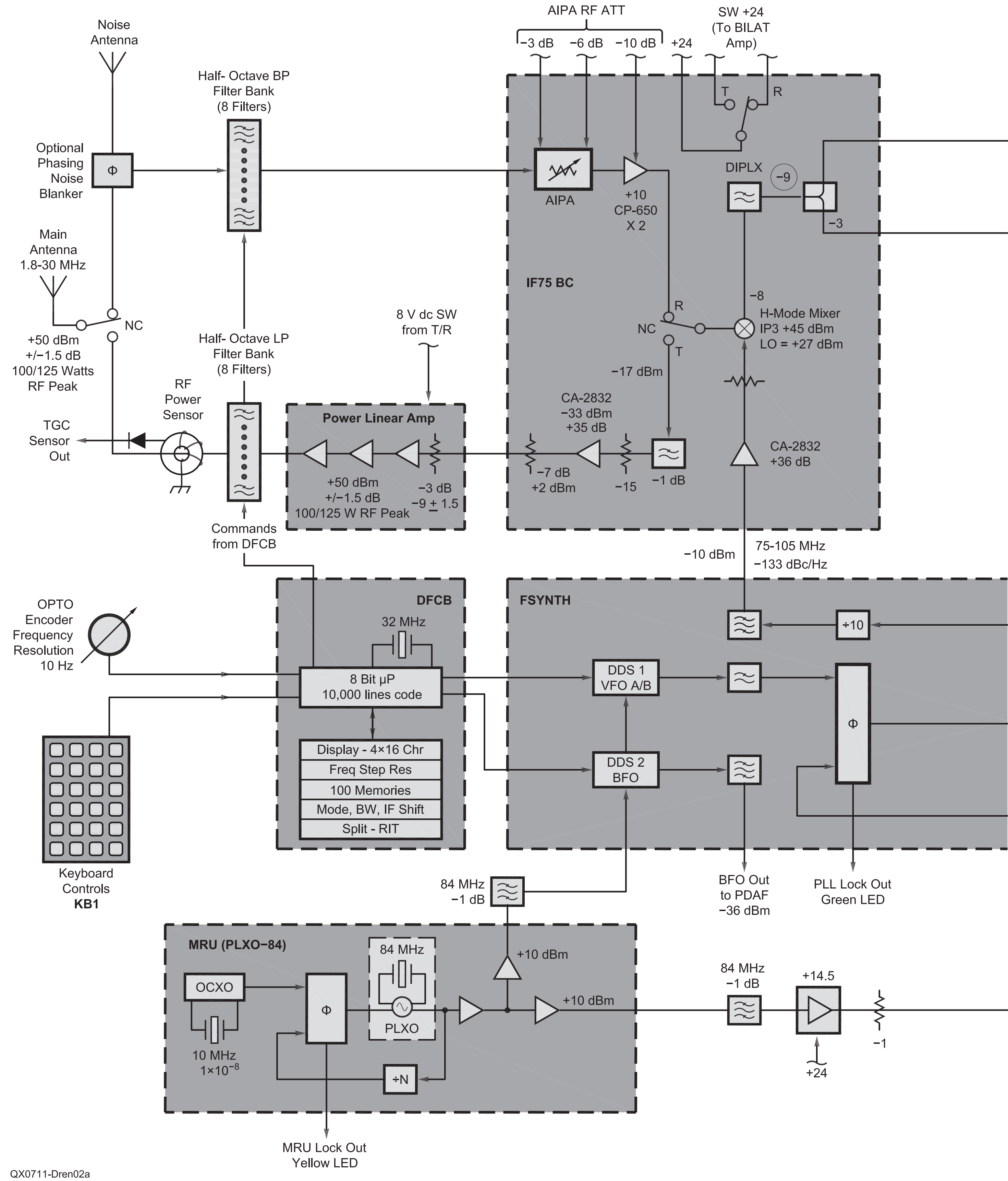
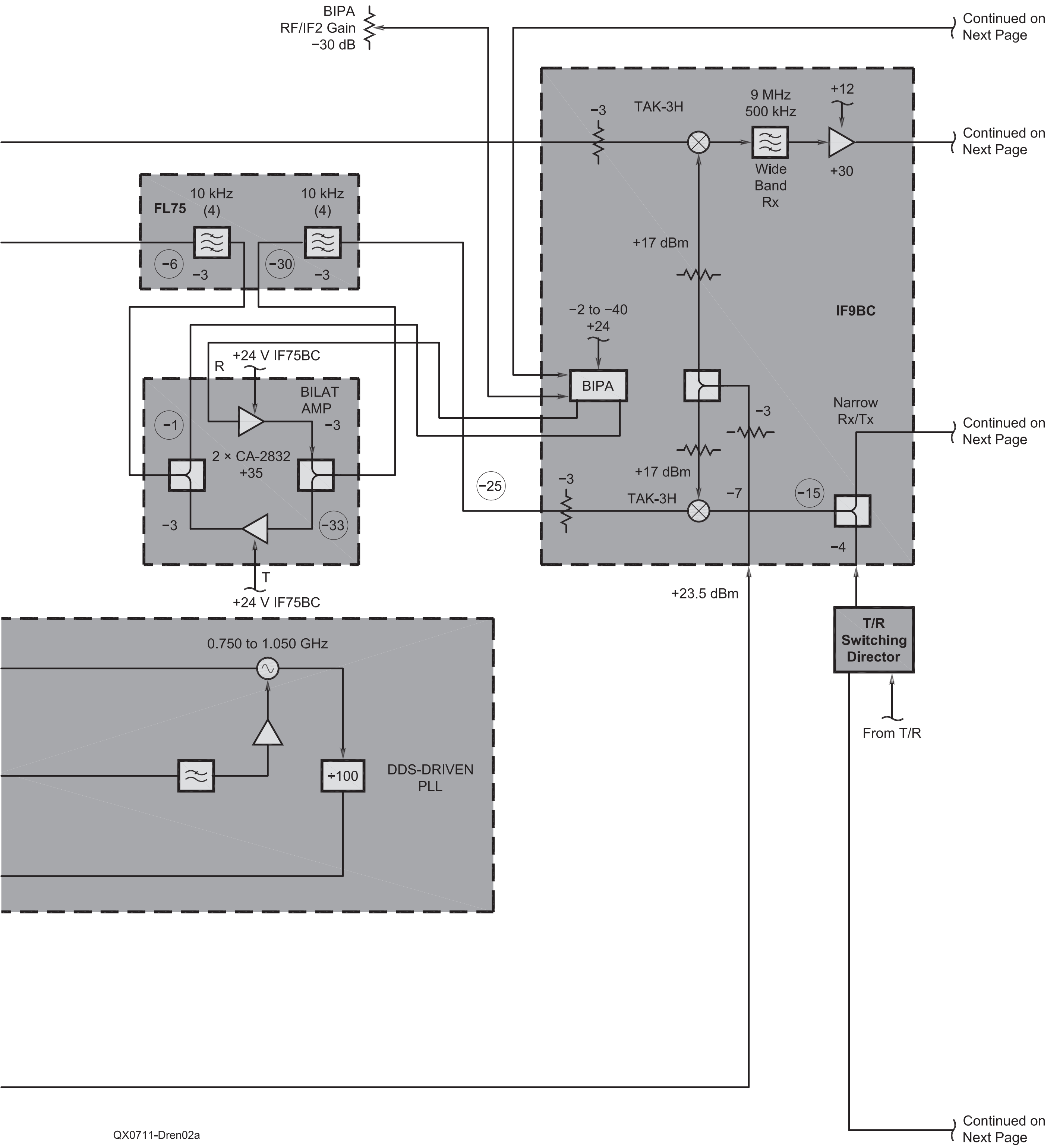


Figure 2 — This block diagram shows the *Star-10* transceiver circuit boards. Note that the diagram continues to three pages.



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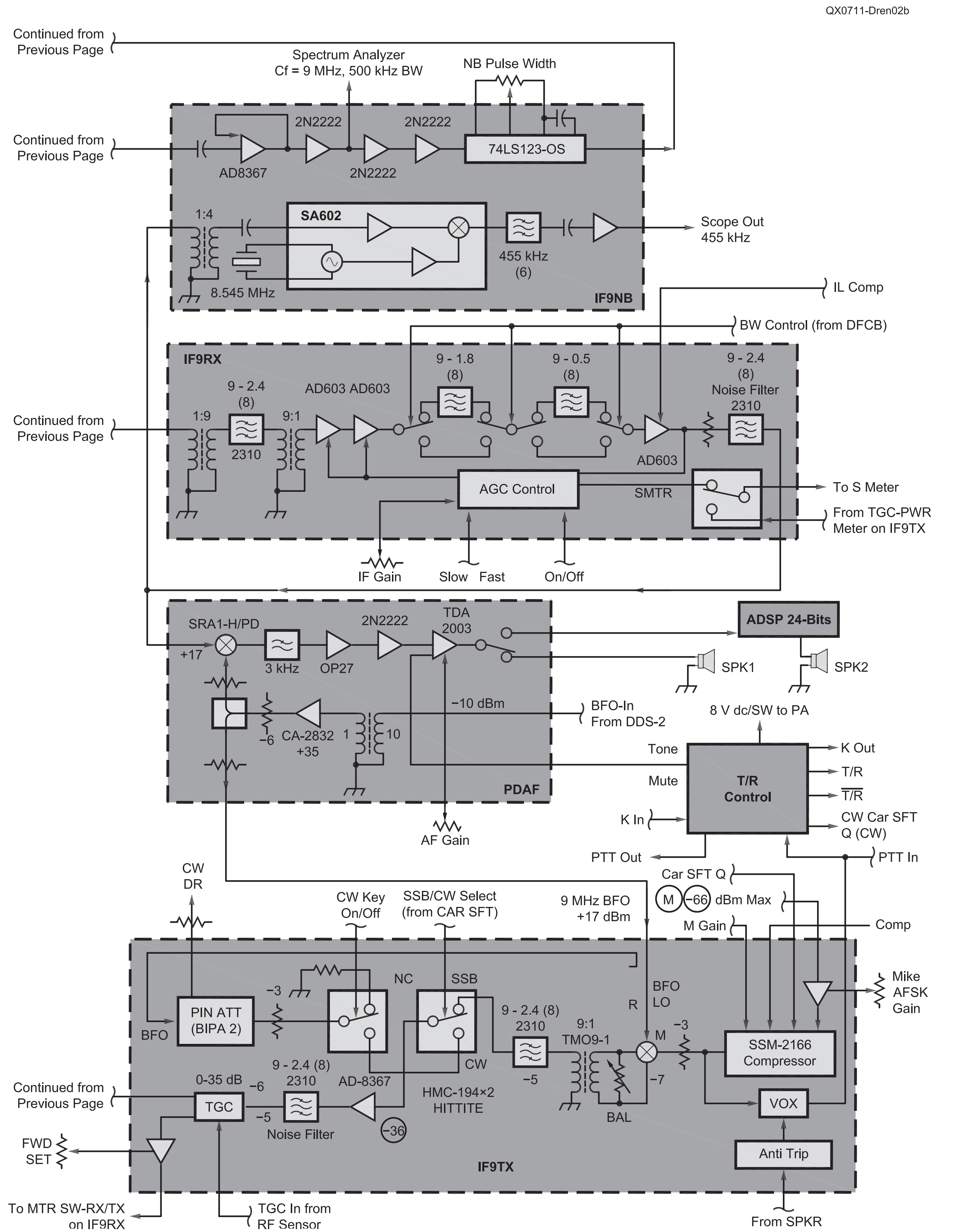

Figure 2 — (continued)

very quiet switching power supply specifically for the *Star-10*.

Design Goals

From the start, the *Star-10* transceiver had two key design goals. The primary goal was to produce a continuous HF coverage system with consistent high dynamic range receiver performance over the entire frequency range that rivals the performance of top of the line equipment. Many receivers today have different performance characteristics at different points in their frequency coverage. The focus of the *Star-10* design was on no-compromise wide-band architecture while maintaining the broadband approach and without accent on unnecessary bells and whistles.

The second goal was to maintain a rigorous and disciplined physical implementation to approach commercial or mil spec grade equipment. These efforts were realized through progressive packaging techniques against the self-imposed system and the circuit design. In addition, the *Star-10* design matured through using ample and gradual trade studies as well as comprehensive design verification techniques and tests consistent with standard engineering processes.

An effort was made to make all interconnecting RF interfaces between assemblies 50 Ω. All RF connectors are gold plated SMA types. RG-194 Teflon and low loss semirigid coaxial cables have been used throughout.

As previously mentioned, the *Star-10* covers seamlessly and continuously the entire HF range of 1.8 MHz to 30 MHz in a single band with a 10 Hz frequency resolution, and with an ultimate receiver composite linear dynamic range of 150 dB or better. (Note: composite linear dynamic range is defined as the ability to funnel a given large input RF signal range into a final transducer without compressing and using multiple AGCs.)

The transceiver is a dual conversion up convert / down convert design that features automatically switched (using miniature RF relays) half-octave filter banks in the front end and a high first IF for superior image, spurious and harmonic rejection over the entire frequency range. Again, there is no channelized single-band-only coverage, like in some of the so-called "high performance" limited coverage 9 MHz IF transceivers found on the market today. The bells and whistles have been limited to the essentials, but plenty of software functionality has been provided throughout. The requirements and specifications for the *Star-10* transceiver are listed below. Dynamic range numbers represent goals as well as final tested results.

System Design

The *Star-10* transceiver features a double conversion approach using a first IF of

STAR-10 ULTRA - HIGH DYNAMIC RANGE COMMUNICATIONS RECEIVER ANALYSIS

System P Input (dBm)	Analysis Temp	AGC 1 ☑ ON		AGC 3 ☑ ON		
-132.00	25 °C	0	10	0	80	Analyze
System P Out (dBm)	**VIEW 600 X 800**	**AGC 2 ☑ ON**		**AGC 4 ☐ ON**		Reset
6.00	SET SIZE TO 75%	0	30	0	0	☐ FALSE Processor Gain 1.00

MDS (dBm)	Linear DR (dB)	ULT BW (Hz)	N Floor (dBm)	Noise Fig (dB)	ICP1dB (dBm)	IIP3 (dBm)	IIP2 (dBm)	System OIM3 (dBm)	SFDR (dBm)
-132.2	34.3	500	-146.9	14.7	-98.0	-93.0	-88.3	-72.0	9.6
Pout (dBm)	**Comp (dB)**	**Gain (dB)**	**N Floor (dBm)**	**SNR (dB)**	**OCP1dB (dBm)**	**OIP3 (dBm)**	**OIP2 (dBm)**	**SFDR3 (dB)**	**SFDR2 (dB)**
6.0	0.0	138.0	5.8	0.3	40.0	45.0	49.7	26.2	22.0

INPUT DEVICE PARAMETERS @ 25°C

	Device Description	Device Gain (dB)	Delta Gain (dB/°C)	Device CP1dB (dBm)	Delta CP1dB (dB/°C)	Device OIP3 (dBm)	Delta OIP3 (dB/°C)	Device OIP2 (dBm)	Device NF (dB)	Delta NF (dB/°C)	Device BW (MHz)
1	FL HO	-1.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30
2	AIPA AGC1	0.00	0.00	99.00	0.00	99.00	0.00	99.00	0.00	0.00	30
3	PREAMP	10.00	0.00	40.00	0.00	45.00	0.00	65.00	5.00	0.00	30
4	HMIX	-8.00	0.00	40.00	0.00	45.00	0.00	65.00	8.00	0.00	30
5	DIPLEX	-1.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30
6	SPLITTER	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30
7	FL75A	-3.00	0.00	10.00	0.00	15.00	0.00	20.00	3.00	0.00	0.01
8	BI-SPL1	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30
9	BIPA AGC2	0.00	0.00	20.00	0.00	15.00	0.00	35.00	0.00	0.00	0.01
10	BI AMP	36.00	0.00	40.00	0.00	45.00	0.00	65.00	5.00	0.00	30
11	BI-SPL2	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30
12	FL75B	-3.00	0.00	20.00	0.00	25.00	0.00	30.00	3.00	0.00	0.01
13	PAD	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30
14	MIX TAK3 H	-7.00	0.00	14.00	0.00	24.00	0.00	30.00	7.00	0.00	30
15	SPLITTER	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	4.00	0.00	30
16	FL9 2.4	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0024
17	IF 9 AGC3	0.00	0.00	99.00	0.00	99.00	0.00	99.00	0.00	0.00	0.0024
18	AD 603 x 2	84.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0024
19	FL9 1.8	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0018
20	FL9 0.5	-6.00	0.00	40.00	0.00	45.00	0.00	50.00	7.00	0.00	0.0005
21	AD 603 FIXED G	20.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0005
22	PAD	-12.00	0.00	99.00	0.00	99.00	0.00	99.00	12.00	0.00	30
23	FL9 2.4	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0024
24	PD SRA1H	-7.00	0.00	10.00	0.00	23.00	0.00	30.00	7.00	0.00	0.0024
25	AF TDA 2003	60.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0024
26	BLANK	0.00	0.00	99.00	0.00	99.00	0.00	99.00	0.00	0.00	100000

CUMULATIVE PERFORMANCE

	Device Description	Gain (dB)	Comp Level (dB)	Signal Power (dBm)	Noise Floor (dBm)	NF (dB)	Cum DR (dB)	IIP3 (dBm)	IIP2 (dBm)	Cum SFDR3 (dB)	Cum SFDR2 (dB)
1	FL HO	-1.00	0.00	-133.00	-146.87	1.00	198.23	100.00	100.00	132.15	99.11
2	AIPA AGC1	-1.00	0.00	-133.00	-146.87	1.00	195.22	96.99	93.98	130.15	96.10
3	PREAMP	9.00	0.00	-123.00	-131.87	6.00	124.23	36.00	55.95	86.15	74.59
4	HMIX	1.00	0.00	-131.00	-139.20	6.67	122.92	35.36	53.05	85.28	72.80
5	DIPLEX	0.00	0.00	-132.00	-140.01	6.86	122.73	35.36	53.01	85.15	72.69
6	SPLITTER	-3.00	0.00	-135.00	-142.78	7.09	122.50	35.36	53.02	85.00	72.58
7	FL75A	-6.00	0.00	-138.00	-144.36	8.51	141.33	20.84	25.62	97.55	75.56
8	BI-SPL1	-9.00	0.00	-141.00	-145.43	10.44	139.41	20.84	25.62	96.27	74.59
9	BIPA AGC2	-9.00	0.00	-141.00	-145.43	10.44	139.20	19.13	24.63	95.13	74.10
10	BI AMP	27.00	0.00	-105.00	-105.36	14.51	130.60	15.52	22.95	90.01	71.22
11	BI-SPL2	24.00	0.00	-108.00	-108.36	14.51	130.60	15.52	22.92	90.01	71.21
12	FL75B	21.00	0.00	-111.00	-111.36	14.51	118.23	3.70	7.41	82.13	63.45
13	PAD	18.00	0.00	-114.00	-114.36	14.51	118.23	3.70	7.41	82.13	63.45
14	MIX TAK3 H	11.00	0.00	-121.00	-121.35	14.52	116.84	3.22	5.38	81.80	62.43
15	SPLITTER	8.00	0.00	-124.00	-124.33	14.54	116.82	3.22	5.38	81.79	62.42
16	FL9 2.4	5.00	0.00	-127.00	-127.31	14.56	122.99	3.22	5.29	85.90	65.46
17	IF 9 AGC3	5.00	0.00	-127.00	-127.31	14.56	122.99	3.22	5.29	85.90	65.46
18	AD 603 x 2	89.00	0.00	-43.00	-43.20	14.67	76.53	-44.00	-39.05	54.36	43.24
19	FL9 1.8	86.00	0.00	-46.00	-46.20	14.67	76.02	-45.76	-43.68	54.01	41.55
20	FL9 0.5	80.00	0.00	-52.00	-52.20	14.67	81.23	-46.11	-45.31	57.49	43.52
21	AD 603 FIXED G	100.00	0.00	-32.00	-32.20	14.67	71.82	-55.53	-53.99	51.21	39.18
22	PAD	88.00	0.00	-44.00	-44.20	14.67	71.82	-55.53	-53.99	51.21	39.18
23	FL9 2.4	85.00	0.00	-47.00	-47.20	14.67	71.70	-55.65	-54.91	51.13	38.72
24	PD SRA1H	78.00	0.00	-54.00	-54.20	14.67	63.61	-58.35	-58.15	49.33	37.10
25	AF TDA 2003	138.00	0.00	6.00	5.80	14.67	34.34	-93.00	-88.28	26.23	22.04
26	BLANK	138.00	0.00	6.00	5.80	14.67	34.34	-93.00	-88.30	26.23	22.02

Figure 3 — Part A: *Star-10* system composite linear dynamic range analysis results anticipate an absolute MDS performance of –132 dBm (–136 dBm was the measured actual result).

75 MHz for good receiver image rejection and a second IF of 9 MHz for achieving ultimate bandwidths of 2.4 kHz, 1.8 kHz and 0.5 kHz. The design allows for baseband DSP to be used after the second conversion. Provisions are made for external spectrum analysis over 0.5 MHz bandwidth at the 75 MHz and 9 MHz IFs. An outboard spectrum analyzer unit can be used for viewing band activity. The entire transceiver's block diagram is shown in Figure 2. This block diagram closely represents the finished product.

As can be seen in Figure 2, the block diagram encompasses both transmit and receive functions. I will focus mainly on the receiver, since the system is bilateral. As can be seen, the receiver system can employ as many as three AGC loops. (Note: A single AGC loop was implemented so far in the hardware, withAIPA and BIPA manually operated). Its behavior was modeled using actual component gains, compression parameters, and ultimate bandwidths, using my specially developed composite dynamic range software entitled Victoria Falls©. This software has the proven capability to ramp up like in real life the input RF at the antenna port all the way from the MDS, up to the system's compression point, turning on all three AGC stages progressively, in reverse order, and graphically displaying the actual dynamic range behavior on a spectrum-analyzer-like color display, proving the entire compression-free composite linear dynamic range performance of over 150 dB.

The results of this analysis are shown in Figure 3A and B. They take into consideration all component parameters shown in the system block diagram from Figure 2. The bottom line composite linear dynamic range results of the analysis are shown graphically in Figure 3C. They anticipate the system's receiver performance from the input to the output as funneled through the system, using the three AGC stages, without compression. (Note: The system's MDS was tested at –136 dBm absolute.) The vertical bands show the three AGC actions necessary to keep the receiver uncompressed over the entire range. Please note how the system's noise figure increases as the RF input is ramped up and the composite AGCs enter the picture. This is normal, as any receiver's noise figure is depreciated by the AGC action, while the signal level is always higher than the receiver's noise figure at any given point on the dynamic range. What is important is that reception is possible with increased noise figure because the signal to noise level is always maintained higher as the signal goes up through the uncompressed dynamic range.

The system design modeling process is usually the most important phase of an entire transceiver design and especially of the receiver design. It is a very tedious process and

STAR-10 ULTRA - HIGH DYNAMIC RANGE COMMUNICATIONS RECEIVER ANALYSIS

System P Input (dBm)	Analysis Temp	AGC 1 ☑ ON		AGC 3 ☑ ON		Analyze
21.00	25 °C	-10	10	-80	80	Reset
System P Out (dBm)	VIEW 600 X 800	AGC 2 ☑ ON		AGC 4 ☐ ON		FALSE ☐ Processor Gain
38.08	SET SIZE TO 75%	-30	30	0	0	1.00

MDS (dBm)	Linear DR (dB)	ULT BW (Hz)	N Floor (dBm)	Noise Fig (dB)	ICP1dB (dBm)	IIP3 (dBm)	IIP2 (dBm)	System OIM3	SFDR (dBm)
-26.9	47.4	500	-146.9	120.0	20.4	25.4	26.5	27.4	18.3
Pout (dBm)	**Comp (dB)**	**Gain (dB)**	**N Floor (dBm)**	**SNR (dB)**	**OCP1dB (dBm)**	**OIP3 (dBm)**	**OIP2 (dBm)**	**SFDR3 (dB)**	**SFDR2 (dB)**
38.1	0.9	18.0	-8.9	47.1	38.4	43.4	44.5	35.0	26.7

	INPUT DEVICE PARAMETERS @ 25°C											CUMULATIVE PERFORMANCE									
	Device Description	Device Gain (dB)	Delta Gain (dB/°C)	Device CP1dB (dBm)	Delta CP1dB (dB/°C)	Device OIP3 (dBm)	Delta OIP3 (dB/°C)	Device OIP2 (dBm)	Device NF (dB)	Delta NF (dB/°C)	Device BW (MHz)	Gain (dB)	Comp Level (dB)	Signal Power (dBm)	Noise Floor (dBm)	NF (dB)	Cum DR (dB)	IIP3 (dBm)	IIP2 (dBm)	Cum SFDR3 (dB)	Cum SFDR2 (dB)
1	FL HO	-1.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30	-1.00	0.00	20.00	-146.87	1.00	198.23	100.00	100.00	132.15	99.11
2	AIPA AGC1	-10.00	0.00	99.00	0.00	99.00	0.00	99.00	10.00	0.00	30	-11.00	0.00	10.00	-146.87	11.00	187.81	99.59	97.61	125.21	92.92
3	PREAMP	10.00	0.00	40.00	0.00	45.00	0.00	65.00	5.00	0.00	30	-1.00	0.01	19.99	-131.87	16.00	124.23	46.00	65.83	86.15	74.53
4	HMIX	-8.00	0.00	40.00	0.00	45.00	0.00	65.00	8.00	0.00	30	-9.00	0.01	11.99	-139.20	16.67	122.92	45.36	62.97	85.28	72.76
5	DIPLEX	-1.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30	-10.00	0.01	10.99	-140.01	16.86	122.73	45.36	62.92	85.15	72.64
6	SPLITTER	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	1.00	0.00	30	-13.00	0.01	7.99	-142.78	17.09	122.50	45.36	62.94	85.00	72.54
7	FL75A	-3.00	0.00	10.00	0.00	15.00	0.00	20.00	3.00	0.00	0.01	-16.00	0.28	4.72	-144.36	18.51	141.33	30.84	35.62	97.55	75.55
8	BI-SPL1	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30	-19.00	0.28	1.72	-145.43	20.44	139.41	30.84	35.62	96.27	74.59
9	BIPA AGC2	-30.00	0.00	20.00	0.00	15.00	0.00	35.00	30.00	0.00	0.01	-49.00	0.28	-28.28	-146.87	49.00	110.84	30.84	35.59	77.23	60.29
10	BI AMP	36.00	0.00	40.00	0.00	45.00	0.00	65.00	5.00	0.00	30	-13.00	0.28	7.72	-105.87	54.00	105.83	30.83	35.52	73.89	57.76
11	BI-SPL2	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30	-16.00	0.28	4.72	-108.87	54.00	105.83	30.83	35.52	73.89	57.76
12	FL75B	-3.00	0.00	20.00	0.00	25.00	0.00	30.00	3.00	0.00	0.01	-19.00	0.30	1.70	-111.87	54.00	105.63	30.63	33.85	73.75	56.92
13	PAD	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	3.00	0.00	30	-22.00	0.30	-1.30	-114.87	54.00	105.63	30.63	33.85	73.75	56.92
14	MIX TAK3 H	-7.00	0.00	14.00	0.00	24.00	0.00	30.00	7.00	0.00	30	-29.00	0.30	-8.30	-121.86	54.01	105.54	30.60	33.38	73.73	56.69
15	SPLITTER	-3.00	0.00	99.00	0.00	99.00	0.00	99.00	4.00	0.00	30	-32.00	0.30	-11.30	-124.83	54.03	105.52	30.60	33.38	73.71	56.67
16	FL9 2.4	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0024	-35.00	0.30	-14.30	-127.81	54.06	111.69	30.60	33.36	77.83	59.75
17	IF 9 AGC3	-80.00	0.00	99.00	0.00	99.00	0.00	99.00	80.00	0.00	0.0024	-115.00	0.30	-94.30	-146.87	115.00	50.75	30.60	33.36	37.20	29.28
18	AD 603 x 2	84.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0024	-31.00	0.30	-10.30	-57.87	120.00	45.75	30.60	33.33	33.87	26.76
19	FL9 1.8	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0018	-34.00	0.30	-13.30	-60.87	120.00	47.00	30.60	33.30	34.70	27.37
20	FL9 0.5	-6.00	0.00	40.00	0.00	45.00	0.00	50.00	7.00	0.00	0.0005	-40.00	0.30	-19.30	-66.87	120.00	52.56	30.60	33.29	38.41	30.15
21	AD 603 FIXED G	20.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0005	-20.00	0.30	0.70	-46.87	120.00	52.56	30.60	33.16	38.41	30.09
22	PAD	-12.00	0.00	99.00	0.00	99.00	0.00	99.00	12.00	0.00	30	-32.00	0.30	-11.30	-58.87	120.00	52.56	30.60	33.16	38.41	30.09
23	FL9 2.4	-3.00	0.00	40.00	0.00	45.00	0.00	50.00	3.00	0.00	0.0024	-35.00	0.30	-14.30	-61.87	120.00	52.56	30.60	33.14	38.41	30.07
24	PD SRA1H	-7.00	0.00	10.00	0.00	23.00	0.00	30.00	7.00	0.00	0.0024	-42.00	0.30	-21.30	-68.87	120.00	52.55	30.60	33.04	38.41	30.03
25	AF TDA 2003	60.00	0.00	40.00	0.00	45.00	0.00	50.00	5.00	0.00	0.0024	18.00	0.92	38.08	-8.87	120.00	47.42	25.43	26.48	34.96	26.75
26	BLANK	0.00	0.00	99.00	0.00	99.00	0.00	99.00	0.00	0.00	100000	18.00	0.92	38.08	-8.87	120.00	47.42	25.43	26.47	34.96	26.74

Figure 3 — Part B: *Star-10* system composite linear dynamic range analysis results anticipate linear performance using all AGCs to +20 dBm. Final performance varied somewhat from this performance, as actual component data changed throughout the design cycle. (See the specifications section in the text.) The program actually ramps up the RF (like in the real life receiver) from the MDS and up through the three AGC ranges (turning them on progressively) until compression occurs.

can take a considerable amount of time. The software used, no matter how sophisticated, can help the designers, but not design the radio for them. This phase of the design is a key part of the design verification methodology mentioned earlier. It sets the system's initial performance goals as close to the final design as possible, so a minimum of modifications will be necessary in the circuit design. Although some designers just string along circuits, no RF system should be pursued without doing this important homework.

With the system's receiver behavior calculated and proven using the software modeling tool, the performance of the design has been further verified and tested (at a final MDS of –136 dBm) in the initial brassboards, and in total concert with the synthesizer's phase noise analysis, brassboarding and tests, which were done separately. A concurrent analysis and breadboarding of the command and control system took place in parallel. Finally, several brassboards and integration of the entire system took place before the final packaging, using all finalized components in progressive order.

A similar analysis was performed in reverse for the transmitting chain, but is not shown here for reasons of simplicity.

With the composite linear dynamic range analyzed, the *Star-10* frequency plan (architecture) was analyzed next, for in-band IF intermodulation distortion (IMD) using my specially designed IMDWEB software. The results of the spurious free performance over the entire 1.8 to 30 MHz range (including receiver image, and higher order spurious products) and using the automatically switched half octave filters are shown in Figure 4A and B. They prove that no significant in-band IF intermodulation distortion products occur at any frequency in the RF frequency coverage with the proper half octave filter switched in,

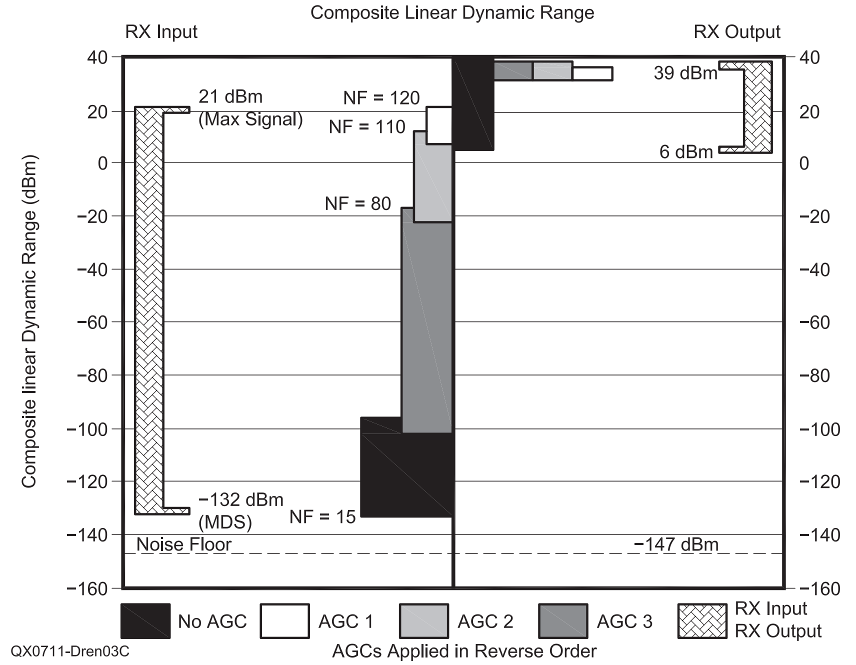

Figure 3 — Part C: Spectrum-analyzer-like graphic results using the software of composite ramping of the RF input over the entire composite linear dynamic range behavior for the *Star-10* system, showing the action of the three AGC stages, and proving the receiver's linear composite dynamic range.

as seen inside the first IF of 75 MHz, and as carried through the second IF of 9 MHz.

Those versed in the art will recognize that this analysis was carried over to a 16th order (8 × 8 harmonics) of products to ensure further reliability (a 7th order analysis is usually sufficient). For a more in-depth explanation regarding how to read IMDWEB charts, see References 1, 5, 6, 7 and 8.

System Description

I will discuss how the *Star-10* transceiver system works. As mentioned before, this will encompass both transmit and receive functions, but I will focus mainly on the receiver, since the system is generally bilateral. Looking at the system block diagram in Figure 2, the antenna is switched between the receiver and transmitter by the T/R control. An optional phasing type noise-canceling noise blanker unit (such as the ANC-4) can be inserted if needed ahead of the receiver to protect against nearby QRN. As expected, the transceiver is always in the receive mode by default.

Figure 4A

IMDWEB Program Input for the *Star-10* System

Corresponding Numbers on Graph of Part B

		1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
Spurs in Band											
MHz/GHz	*Frequencies*	*Band 1*	*Band 2*	*Band 3*	*Band 4*	*Band 5*	*Band 6*	*Band 7*	*Band 8*	*IF2*	*IF3*
F2 (RF)	Cf	2.5	3.5	5	7	10	14	20	27	75	9
	BW 1	1	1	2	4	4	4	6	6	0.5	0.1
	BW 2	0.25	0.25	0.5	1	1	1	1.5	1.5	0.1	0.01
	BW 3	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.01	0.01	0.003
F1 (LO)	Cf	77.5	78.5	80	82	85	89	95	102	84	8.545
F OUT (IF 1)	Cf	75	75	75	75	75	75	75	75	9	0.455
	BW 1	2	2	2	4	4	4	5	6	0.5	0.1
	BW 2	1	1	1	1	1	1	1	1	0.1	0.01
	BW 3	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.01	0.003

Figure 4 — Part A: IMDWEB program inputs for the *Star-10* system. The data is coded and keyed with the graphic results at Part B.

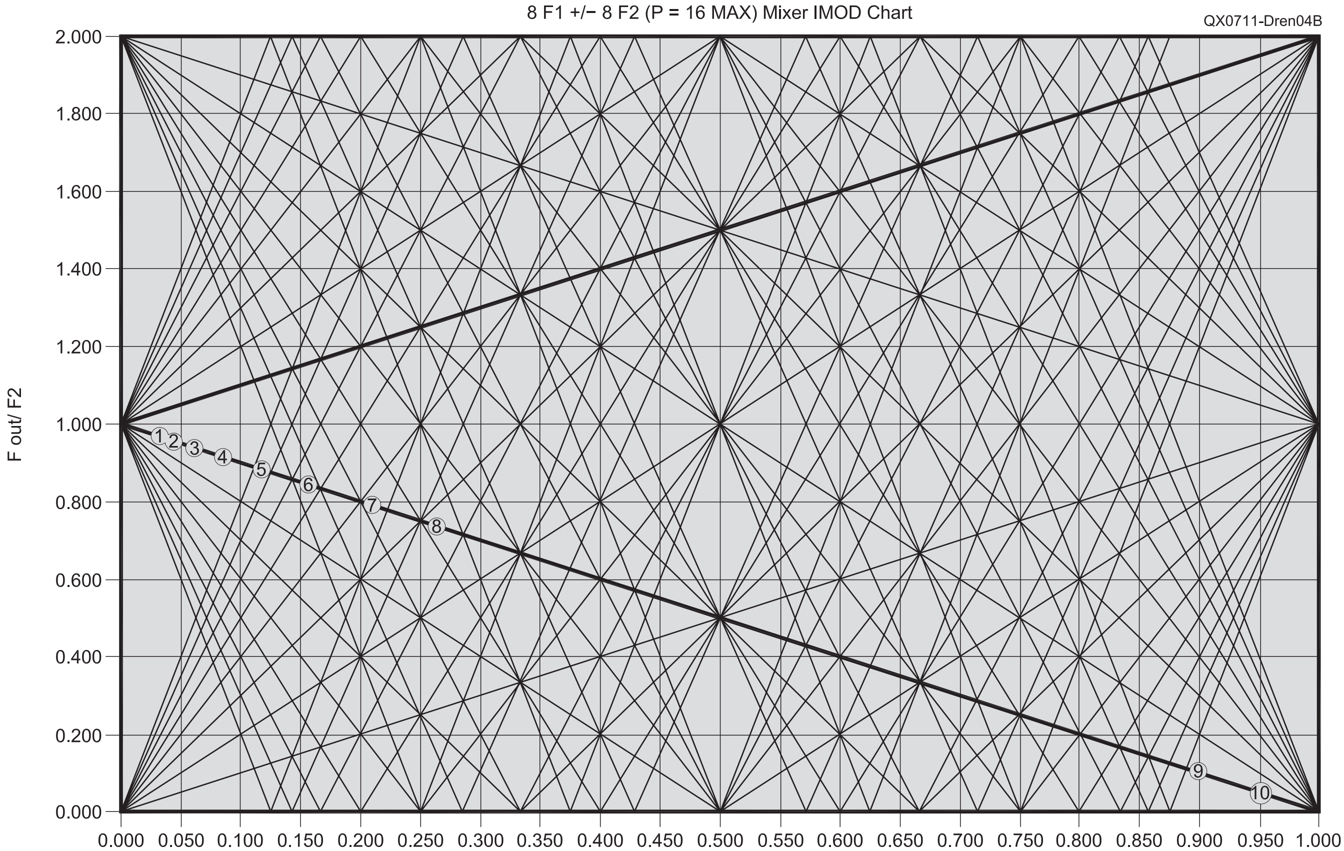

Figure 4 — Part B: The IMDWEB program final results clearly prove that no in-band IF intermodulation product (IMD) lines cross the IFs (the small numbered circles) anywhere in the frequency coverage. The complex IMD results are carried to a 16th order, and show good performance throughout the system's conversions. The frequency ranges are coded to Part A to show the entire system performance in a single plot.

As previously mentioned, the *Star-10* features independent, automatically switched half-octave filter banks for receive and transmit. This is shown at the top left of Figure 2. In the receive mode, RF signals from 1.8 to 30 MHz are automatically selected by the command and control mechanism in the half-octave receiver band-pass filter bank by the DFCB (Command and Control) board as shown, depending on the frequency of operation. The same commands are presented in parallel to a set of high power half-octave low-pass filter banks that have corner frequencies matching exactly the receiver's half-octave filters.

The actual implementation of the automatically switched half-octave receive and transmit filter banks will be discussed in greater detail later.

Automatic frequency selection is achieved anywhere in the frequency range of 1.8 to 30 MHz, providing equal image and spurious rejection in receive, as well as equal harmonic and spurious rejection in transmit anywhere in the frequency coverage.

The 75 MHz first IF puts the receiver image away by 150 MHz at any frequency between 1.8 to 30 MHz. With the proper half-octave filter selected in the banks, the amount of rejection provided is uniform throughout the coverage. Conversely, the proper half-octave low-pass filter selected in the transmit chain insures equal spurious and harmonic rejection throughout the frequency range. (See References 1, 2 and 5.)

Consequently, both receiver and transmitter filter functions are exactly identical, unless operating split over a wide range, in which case appropriate switching between the selected frequencies occurs over the range upon T/R switching. The selection is automatically achieved from the command and control board (DFCB), which also controls the synthesizer (FRU) commands.

The filtered received RF signals from the half-octave bandpass filter bank enter the receiver circuits in the IF75BC board assembly through the advanced intercept point attenuator (AIPA) and the +10 dB push-pull preamplifier located on this board. This combination allows for the programmable AIPA attenuators (part of the AGC control system) to be inserted in the receiver front end. Because of the tremendous dynamic range capability of the *Star-10*, the preamp can be always on. The AIPA functions are implemented via miniature RF relays. Conversely, the transmit chain, when activated, outputs RF signals to the power linear amplifier and further to the high power automatically switched half octave low-pass filter banks, through the RF power transmitter gain control (TGC) and further through the T/R switch, to the antenna.

The front end of the *Star-10* transceiver, IF75BC sets the dynamic range of the entire system as mentioned before. Class A amplifiers operating at 24 V are used in conjunction with a low-noise, high-intercept-point FET push-pull preamplifier using the CP 650, the programmable front end attenuator switched with RF relays, a special high level (class III) H-mode mixer and other hardware. The IF75BC assembly dissipates about 30 W of dc power to insure the high dynamic range for the receiver. Two brushless miniature fans extract heat from the amplifiers through heat sinks. The board is housed in a machined aluminum box with cutouts for command

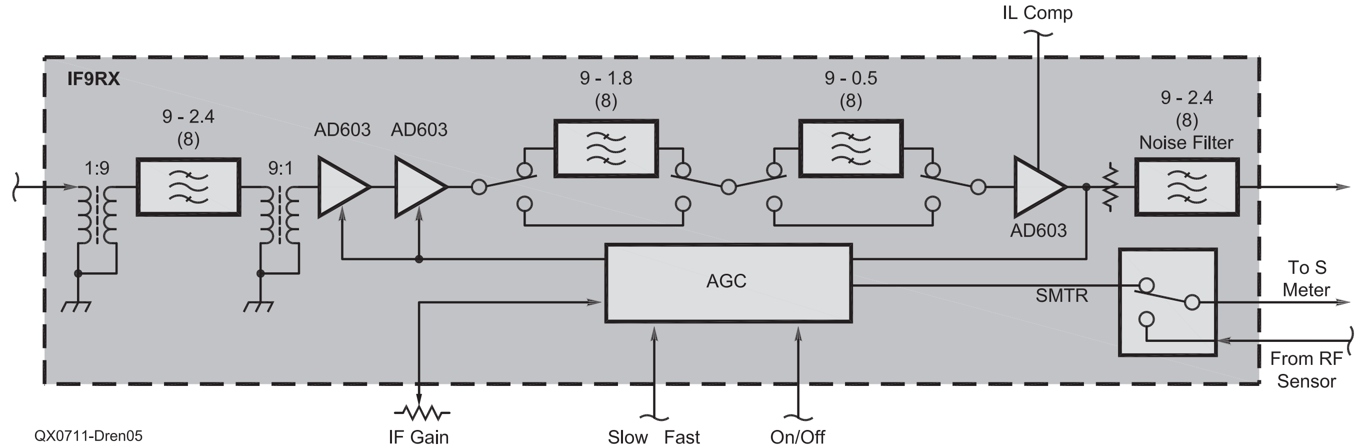

Figure 5 — IF9RX uses a cascaded filter selection of the ultimate receiver bandwidth, depending on mode and bandwidth (wide or narrow) choice, as commanded by the command and control (DFCB) and keypad assemblies.

and control connectors and SMA connectors for the RF ports.

The IF75BC assembly creates the first IF at 75 MHz and works in receive as well as transmit. It also contains a low-pass filter and diplexer-splitter circuitry. Part of the 75 MHz IF information is directed to the crystal-roofing filter for further processing. The other half, which is 500 kHz wide, is directed to the IF9BC board for further conversion and to IF9NB for spectrum analyzer and noise blanker functions.

The 75 MHz roofing filter is bilateral and is made of two, four-pole sections with a 3 dB bandwidth of ~10 kHz. These filters have been expressly designed for the *Star-10*. They exhibit high intercept points and can withstand the RF levels (up to +5 dBm) present in the system at this point in the receiver system over the entire dynamic range. For better signal handling, the roofing filters have been distributed before and after the bilateral amplifier assembly BILAT AMP, as shown.

The 75 MHz roofing filter assembly is followed by the bilateral amplifier (BILAT AMP) assembly. This assembly allows 75 MHz signals to pass automatically either way (receive or transmit) by merely switching the 24 V power distribution to it from IF75BC, which in turn is performed by the T/R assembly. The circuit is unique because there is no need for hard switching of RF inputs and outputs, due to the automatic rejection of unwanted RF paths provided by the natural isolation of the unused sides of the splitters/combiners at the input and output of the amplifiers. The BILATAMP amplifiers are high gain (+36 dB), high intercept, class A types similar to those used in the IF75BC assembly. A similar brushless miniature fan is used for cooling here. Only one amplifier is on at a time, allowing for cooler operation. The *Star-10* makes ample use of passive splitters and combiners for its bilateral circuitry. The paths not used provide some 30 dB of natural isolation to the used paths. Additional switching has been found necessary in addition to this isolation to provide complete muting in the IF9RX circuitry.

The FL75 roofing filters and BILAT AMP assemblies are followed by the IF9BC assembly. This assembly is equipped with the second AGC loop, called BIPA, which allows for 30 dB of adjustable gain action from the front panel RF/IF gain control. The adjustable BIPA attenuator as well as the transmit CW drive circuits use a classic PIN attenuator circuit, which will be discussed later. The 75 MHz IF signals coming from the BILAT AMP assembly are coverted here to the 9 MHz IF (500 kHz wide IF) for the IF9NB and for the main 9 MHz receive IF assembly called IF9RX.

In addition, the 9 MHz transmitter IF, IF9TX, is also input to the IF9BC assembly using a similar passive splitter/combiner technique as previously used in the BILATAMP. The IF9BC assembly uses high-level class II mixers to perform the conversions. A 500 kHz wide, 9 MHz IF filter is used to condition the spectrum analyzer and noise blanker functions of the IF9NB. The ultimate bandwidth for the receiver is established through the crystal filter bank in the IF9RX assembly. The bandwidth for the SSB/AFSK transmit functions is established through a similar filter bank in the IF9TX assembly.

As can be seen from Figure 2, the IF9BC main receiver output is further input to the IF9RX assembly. This IF achieves the ultimate receiver bandwidth selection and amplification as commanded by the command and control assembly DFCB. The IF9RX board provides 100 dB of gain (80 dB AGC) using three high dynamic range (high IP3) logarithmic/linear IF blocks from Analog Devices. The IF bandwidth selection is provided by four 8-pole crystal filters that were specially designed for the *Star-10*. Instead of selecting individual filters like conventional IF designs, the *Star-10* IF9RX filter assemblies are combined in a cascaded AND function (rather than an OR function) for a total of 32 poles (plus the 8 pole roofing filter) of superb selectivity. This cascaded architecture makes the IF9RX a unique design that works in tandem with the system's command and control software. This is shown in Figure 5.

The eight pole crystal filters are configured in a cascaded configuration for increased selectivity for a minimum of 16-pole and a maximum of 32-pole selectivity (in addition to the 8 pole roofing filter). The first and last 2.4 kHz filters set the maximum IF bandwidth of 2.4 kHz while the 1.8 kHz and 500 Hz filters set narrow selections for different modes depending on the mode selected from the command and control. Three AD603 logarithmic linear amplifiers are used to provide ~100 dB of gain (80 dB AGC), with the third amplifier used to compensate for narrow filter insertion loss and equal AGC/S-meter indications regardless of the filter combination. The last 2.4 kHz filter is used to clean up noise from previous amplifiers.

As shown in Figure 5, two 8 pole crystal filters with a bandwidth of 2.4 kHz are always used at the beginning and the end of the 9 MHz IF chain for good noise management. Then, additional 8 pole crystal filters of narrower bandwidths are inserted or removed between the gain stages (for a maximum of 32 poles in CW Narrow) depending on the mode selection and as commanded by the DFCB. The selection is achieved with miniature RF Teledyne relays, just as in the front end of the radio (no PIN diode switching for RF paths in this radio). Automatic insertion loss compensation control is achieved depending on the diverse filters configurations so there is no difference in signal amplitude when changing filters and bandwidths.

Because of the 100 dB gain provided by this important board, and the limited board size of 5.5 × 4.5 inches, the IF9RX board had to be specially laid out to prevent possible oscillation. The first layout did oscillate. A special effort was made by KD7KEQ to provide a new layout, using hundreds of plated through ground stitches in the double-sided board ground planes, to make the system as quiet as technically possible. Additional effort was put into its execution of this board by KG6NK, making this demanding board perform, as it should.

Conversely, the IF9TX assembly provides for processed SSB signals and all other transmit functions supplied to the IF9BC. Microphone amplification and compression are provided together with SSB mixer, CW drive, carrier insertion, transmitter gain control (TGC) feedback, and switching functions using Hittite solid-state RF switches. In addition, SSB transmit bandwidth and on the air "sound character" are set by two crystal filters for a total of 16 poles of 2.4 kHz bandwidth, similar to those in the IF9RX. This allows for a true and clean communication sounding SSB transmission.

Finally, the receiver chain is completed by feeding the IF9RX output to the product detector PDAF assembly. Here, the 9 MHz coherent BFO signal coming from the synthesizer (FRU) enters the product detector mixer using a high level class II device, to be demodulated by the mode commands received from the DFCB assembly. The BFO frequencies used by the product detector are shown in Table 1, along with all other LO interactions for setting up the system in all the available modes of operation. The functions are entered through the KB1 keyboard, processed through the DFCB and output by the FSYNT assembly. As can be seen, the commands change with the T/R functions, so the net result is that we transmit exactly on the same frequency as we receive, regardless of the operating mode. The functions are selected automatically by DFCB and are subject to the modes selected.

The filtered and AGC conditioned IF9RX output is finally presented to the PDAF product detector assembly. Here, the 9 MHz signals from the IF are mixed in a high-level class II mixer (the product detector) with the high level (another class A amplifier is used here) BFO LO signal coming from the coherent synthesizer FSYNT. An audio low-pass filter further cleans up the resulting audio signal before being amplified and output to the DSP and/or speaker. Additional audio beeps corresponding to commands coming from the command and control assembly DFCB are audio mixed and presented to the audio stages. Muting signals from the T/R assembly are fed concurrently to PDAF and IF9RX as well as to other points in the receiver chain.

In addition to the muting function, the T/R assembly combines conditioned keying and PTT/VOX signals received through the command and control assembly DFCB, to perform the total transceiver control functions. For example, the T/R uses a unique method of digitally generating slight delays (the Morse code is shifted through a shift register) in the CW keying path, to allow the synthesizer to settle and lock in QSK, before Morse code characters are shifted out through the transmitter. This helps to stop possible chirping when using the extra wide split frequency capability of this transceiver and also between Morse code elements, making for clean CW if operating on two separate frequencies, and even between the elements of CW signals. The T/R assembly is fully digital and will be discussed later.

We will now discuss the command and control DFCB assembly in conjunction with the frequency reference unit (FRU) FSYNT assembly, along with the master reference unit (MRU) assembly.

The heart of the *Star-10* is the command and control assembly DFCB, which works in conjunction with the keypad assembly and the RS-232 interface. These assemblies are physically installed together with the displays behind the front panel of the transceiver as shown in Figure 2. The transceiver's entire capability is slaved to a powerful 8-bit Microchip PIC-17C44 microprocessor controller that runs approximately 10,000 lines of code continuously at 32 MHz (Note: chosen above the HF range to keep possible spurious RF products out of the receiver's input range) in a closed loop, only to be interrupted by its keypad or RS-232 commands.

I initially used the UV erasable PIC-17C44 version, offered in the in-line package for optimal prototype development. This allowed for multiple UV erasable reprogrammed software versions (at least 100 revisions) with the latest V.3.1.

A Few Words About The Chosen Microprocessor

The PIC-17C44 microprocessor operates at up to 33 MHz with full interrupt capability. I am using it at 32 MHz to put any possible spurious problems above the HF band. The PIC-17C44 has an instruction cycle of 125 ns. It is equipped with 33 I/O ports (all have been used), and 16 levels deep hardware stack plus 64K × 16 addressable program memory space.

The PIC-17C44 microprocessor is a high speed CMOS, fully-static protected, 8-bit microcontroller employing an advanced RISC architecture. It has enhanced core features, 16-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 16-bit wide instruction word with a separate 8-bit wide data word. The two-stage instruction pipeline allows all instructions to execute in a single cycle. A total of 55 instructions (reduced instruction set) are used. Additionally, a large register set gives this microprocessor some new architectural innovations used to achieve a very high performance. For mathematically intensive applications such as used in this application, the device has a single cycle 8 × 8 Hardware Multiplier.

PIC-17C44 microcontroller typically achieves a 2:1 code compression and a 4:1 speed improvement over other 8-bit

Table 1

Effects of Mode Selection on System Frequency Compensation of Local Oscillators

This includes the BFO (LO3) in the PDAF provided by the FSYNT, and as commanded by the Command and Control board, DFCB and the Keypad.

MODE	*LO1 RX*	*LO1 TX*	*LO2 RX/TX*	*LO3 RX*	*LO3 TX*	*SHIFT/RX-TX*
USB	UP 1500 Hz	UP 1500 Hz	84 MHz	8.9985 MHz	8.9985 MHz	1500 Hz
LSB	DWN 1500 Hz	DWN 1500 Hz	84 MHz	9.0015 MHz	9.0015 MHz	1500 Hz
CWU	UP 800 Hz	UP 800 Hz	84 MHz	8.9992 MHz	9.000 MHz	1500 Hz
CWL	DWN 800 Hz	DWN 800 Hz	84 MHz	9.0008 MHz	9.000 MHz	1500 Hz
FSKU	UP 2210 Hz	UP 2210 Hz	84 MHz	8.99779 MHz	8.99779 MHz	NA
FSKL	DWN 2210 Hz	DWN 2210 Hz	84 MHz	9.00221 MHz	9.00221 MHz	NA

microcontrollers. The PIC17C44 has up to 454 bytes of RAM and 33 I/O pins. In addition, the PIC17C44 adds several peripheral features useful in high performance applications including (not all utilized in this application):

- Four timer/counters
- Two capture inputs
- Two PWM outputs
- A universal synchronous asynchronous receiver/ transmitter (USART)

These special features reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. We will discuss the command and control DFCB assembly later.

The *Star-10* has been designed with a very flexible and friendly human interface that has been compared with the feel of classic HP test equipment. This functionality did not come easy and has taken a considerable amount of time and dedication to design and prove. I spent approximately a year and a half in the complex system and command interface requirements and implementation, investment that resulted in a "bug free" design.

The command and control interface DFCB was designed using on board EEPROM

Command and Control Calculations

One of the main governing equations for the front panel display is:

$$f_{Display} = \frac{(f_{LO} - f_{IF})}{10}$$

As an example, for an f_{IF} of 75,000,000 Hz (75 MHz) and a local oscillator output of 89,240,110 Hz, the control software will calculate the operating frequency to display:

$$f_{Display} = \frac{(89{,}240{,}110 - 75{,}000{,}000)}{10}$$

$$f_{Display} = 14{,}240{,}110$$

In this case, the *Star-10* display will show 14.240.11, representing an operating frequency in the 20 m band. Figure A shows the relationships between these various signals as they are processed.

There are, of course, many other calculations taking place in the Command and Control assembly. The following are a few examples of calculations related to how the microprocessor deals with the tune frequencies as related to the DDS.

$$f_n = \left(\frac{2^{32}}{100 \times 10^6}\right) \bullet \left(\frac{75 \times 10^6 + Display}{10}\right)$$

$$f_n = \left(\frac{2^{32}}{100 \times 10^7}\right) \bullet 75 \times 10^6 + \left(\frac{2^{32}}{100 \times 10^7}\right) \bullet Display$$

Where f_n is the Tune Value.
Then:

$$f_n = 322122547.2 + 4.294967296 \bullet Display$$

For example, a Display value of 29.999990 × 10^6 yields:
$f_n = 450971523$

$$DDS_{OUT} = \frac{f_{Desired} + f_{IF}}{10}$$

And

$$DDS_{OUT} = \frac{DDS_{Word} \bullet f_{REF}}{2^{32}}$$

Let

$$f_{KBD} = \frac{f_{Desired}}{10}$$

$$\frac{DDS_{Word} \bullet f_{REF}}{2^{32}} = f_{KBD} + \frac{f_{IF}}{10}$$

$$DDS_{Word} = \frac{2^{32}}{f_{REF}} \bullet f_{KBD} + \frac{2^{32}}{f_{REF}} \bullet \frac{f_{IF}}{10}$$

Let

$$f_{REF} = 84 \times 10^6$$

$$f_{IF} = 75 \times 10^6$$

Then

$$DDS_{Word} = 51.13056304762 \bullet f_{KBD} + 383479222.8571$$

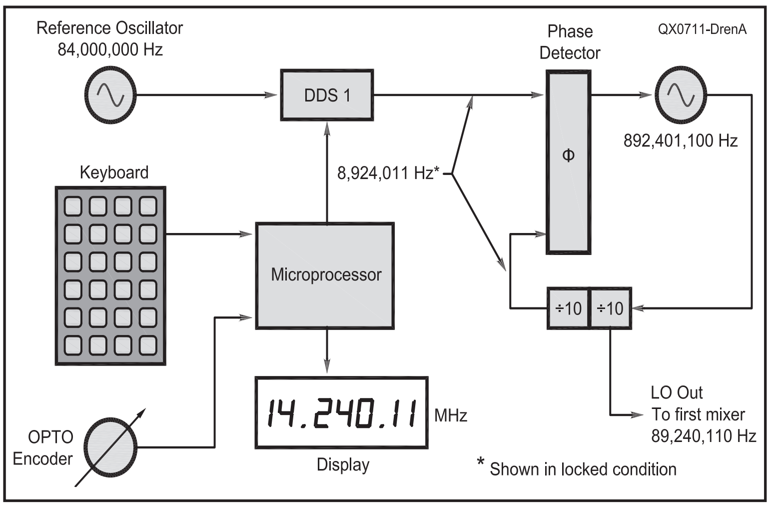

Figure A — This partial block diagram shows a simplified version of the frequency generation section of Figure 2. This diagram illustrates how the microprocessor and 84 MHz reference frequency control the DDS1 signal going into the PLL phase detector as well as displaying the radio operating frequency. The PLL output is the LO signal to the first mixer.

memory. I/Os were implemented through the custom keypad (which was built from scratch) as augmented by an opto-encoder. Up, down and direct frequency inputs, mode select, bandwidth select, split, RIT and IF Shift memory functions are addressed directly from the keypad and the opto-encoder. The opto-encoder (main knob) also has a push-push function to select two brightness levels for the integrated display and the sound feedback signals are audible through the audio amplifier.

The *Star-10* system power up default is 10.00000 MHz — WWV-USB mode, for zeroing the entire system's accuracy from the MRU. Upon turning on the power, the display shows 10.00000 MHz along with the *Star-10* logo and the software version (V.3.1). The receiver is set up by default to USB and if an antenna is connected, WWV signals are heard for initial calibration. After this imposed calibration on the system (at each power up), the operator inputs a new operating frequency to the last 10 Hz via the keypad. See the lead photo for a picture of this keypad. There are no "bands" on the keypad. This transceiver is programmable from 1.8 MHz to 30 MHz in one band, with 10 Hz resolution. The front end filtering selection is executed seamlessly and follows automatically behind the scene through the automatic switching half-octave filter banks.

The main display is facilitated through two 32-character, back-lit, green-blue integrated LCD-Twist dot matrix displays. (Note: this provides a total of 64 characters on 4 lines.) Slight frequency changes and RIT/IF-SHIFT intervention are achieved via the opto-encoder in conjunction with the keypad as the human interface. In addition, the main knob activates brightness and sound functions through the microprocessor.

One of the key functions of the command and control assembly is to control the frequency synthesizer (FRU), FSYNTH. This unit uses two coherent loops in conjunction with the MRU reference operating at 84 MHz, which is also used as a fixed second LO. (See References 9 and 10.) There are two AD-9850 DDS circuits to be controlled. The first DDS is used in a microwave DDS-Driven PLL (see Reference 10) system that was previously described in References 3 and 4. This loop operates in 1 Hz increments from approximately 0.7 GHz to 1.05 GHz and is divided by 10 for improved phase noise performance for the first variable LO. The highly filtered second DDS is used as a 9 MHz BFO providing the various product detector frequencies from Table 1. The 84 MHz MRU LO serves as both, a reference for the two DDSs as well as a fixed LO for the second conversion. Thus, a fully coherent system results.

The command and control DFCB system is capable of addressing either the main loop DDS or the BFO DDS. The main synthesizer loop (the DDS-Drive PLL microwave loop) is controlled through direct keypad entry as taken over by the opto-encoder. When in the mode select mode, the keypad controls the microprocessor such that the BFO/DDS-2 follows a fixed programmed function/frequency offsets from the nominal 9 MHz and as changed by the USB, LSB, CW, CWN, AFSK command requirements. This programmability along with the entire transceiver's frequency sources programmability was previously shown in Table 1.

Up/Down arrow commands are used on the keypad to enter RIT and PBT offsets. The passband function (marked "SFT" on the keypad) allows selected TX or RX offsets to vary ± 1.5 kHz moving the IF BW and other sources in either side of the zero in either transmit or receive. Once set, the IF PBT remains memorized during the power-on session, to be reset to its nominal values by the power "off" switch until the next power-on session begins and a new "SFT" entry is input. The RIT function allows for ± 9.9 kHz received frequency offset from nominal and gets reset to nominal zero with transceiver power off.

After the power up and the 10 MHz calibration mode appears, the operator enters the frequency of interest via the keypad in VFO A. This frequency is the receive and transmit frequency for the transceiver, unless choosing to operate split. It can be fine tuned with the main tuning knob or the up/down arrow buttons, with addressable resolution as well as by the RIT and PBT keypad inputs. If choosing to hold either the UP or the DWN buttons for more than a second, a scanning function from the nominal displayed frequency is achieved. Touching any other keypad button can stop the scanning. By pushing the split button on the keypad, a second frequency, VFO B can be entered within the transceiver's entire frequency coverage. The new frequency (VFO B) shows up on the second row of the frequency display as shown in the lead photo. The R>T and A>B buttons change/reverse the addressability of the two VFOs.

VFOs A and B are virtual VFOs, since the same synthesizer is used to generate them. Hams are usually taught to think that there are actual separate VFOs in synthesized radios. In reality, this is far from truth. The virtual VFO functionality using a single synthesizer is much the same here as in most synthesized transceivers on the market today.

Additional keypad inputs MODE and W/N keys select the mode and bandwidth requirements. These functions automatically correct the LO settings, so bandpass frequency centers and appropriate bandwidths are selected in the IF9RX and IF9TX to provide seamless operation on the exact same frequency with the station at the other end.

More flexibility is provided through a linear scale frequency indicator showing on the last row of the display as shown. This is visible in Figure 2. The DFCB also provides for scanning functions as well as 99 memories. Finally, the keypad can be totally locked up through the LCK function button.

The frequency synthesizer (FRU) DDSs are commanded by DFCB through serial communication lines. The serial communication speed is sufficient to allow for a proper human interface. Access time is in the microseconds after the microprocessor has been speeded up to the 32 MHz closed loop operation. It should be noted that initial microprocessor clock speeds were progressively increased from the initial 4 MHz to the current 32 MHz as the system grew in complexity. As we did not initially know what size software we would end up with, running approximately 10,000 lines of code in a continuous loop proved to be too slow for interrupt interaction compatible with human operator reactions. Thus, the 32 MHz resulted. The DFCB uses its own crystal oscillator. Some of the governing formulas for the system's interface are shown in the sidebar.

The DFCB commands are presented to the synthesizer, FSYNTH. The synthesizer translates these commands into variable and fixed frequencies using the DDSs and the microwave loop operating from 0.75 GHz to 1.05 GHz as locked to the fixed 84 MHz crystal reference of the MRU (master reference unit). The MRU is a separate assembly. It uses a tight tolerance, 0.001% quartz crystal in a Colpitts PLXO (phase locked crystal oscillator) circuit to provide a close-in phase noise performance of better than –165 dBc/Hz. The 84 MHz crystal is further locked in the MRU to a 10 MHz oven controlled crystal oscillator (OCXO), which provides the long-term stability of 1×10^{-8} for the entire radio, after a 30 second warm-up time. The 10 MHz source is for high stability, while the 84 MHz source is to insure good phase noise performance. The MRU is powered up once and could be left on even during transceiver power off. In the present implementation, it is powered together with the rest of the radio. Its warm-up time (which is the radio's warm-up time to 1×10^{-8}) is 30 seconds. A more detailed description of the MRU will be presented later.

The MRU frequency is used to reference the two DDSs in the FRU, as well as serves as the second fixed LO for the radio. A single high purity microwave VCO is used in the microwave PLL of the FRU. The synthesizer description and operation has been presented in References 3 and 4. After continued improvements in the loop bandwidth versus lock-up trade offs and additional dc filtering, a –133 dBc/Hz close in phase noise performance has been realized at the LO1 injection point. This performance will be discussed further in Part two of the series. As phase noise translates directly into the system IFs on a dB per dB bases, this performance is fully compatible with the MDS and dynamic range expected of the receiver. Comprehensive DR tests against top of the line transceivers were made in the KG6NK laboratory using state-of-the-art test equipment. More on this performance will be presented later.

This concludes Part 1 of this article. In Part 2, I will discuss major assemblies and circuit design/development issues for the *Star-10* transceiver blocks. Pictures and operational discussions of the blocks will also be introduced. Total system integration and performance tests will also be presented in this series.

Cornell Drentea, KW7CD, took his first radio receiver apart (and put it back together) at the early age of six. He has been a ham since 1957. Since then, he's built many radios and transceivers and made his passion for designing "radios" his lifelong profession. As an Amateur Radio operator, he is known for his extensive RF technology articles in magazines such as ham radio, Communications Quarterly, RF Design, *and* QEX.

Professionally, Cornell is an accomplished RF technologist, an engineer and a scientist with over 40 years of hands-on experience in the aerospace, telecommunications and electronics industry. He has been involved in the design and development of complex RF, radar, guidance and communications systems at frequencies of up to 100 GHz. Cornell has developed several state-of-the-art RF products including ultra wide band high probability of intercept microwave receivers, complex synthesizers, multi-modulation transmitters, Doppler agile space transceivers as well as high power RF linear amplifiers. He received his formal education abroad with continuing studies and experience achieved in the United States.

Cornell has presented extensively on RF design topics at technical forums such as IEEE, RF-Expo, Sensors-Expo and has given comprehensive professional postgraduate courses in RF receiver design, synthesizer design, sensors and communications. He has published over 80 professional technical papers and articles in national and international magazines. He is the author of Radio Communications Receivers, *McGraw Hill, ISBN 0-8306-2393-0 and ISBN 0-8306-1393-5, 1982, and holds five patents. He is currently available for consulting to large and small RF enterprises. You can find out more about Cornell, his consulting and his RF course offering entitled* The Art of RF System Design *on his Web site:* **http://members.aol.com/cdrentea/myhomepage/**

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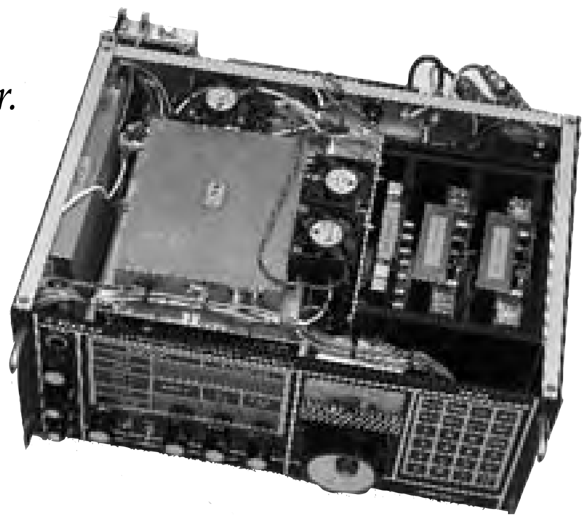
QEX

Cornell Drentea, KW7CD

cdrentea@aol.com

The *Star-10* Transceiver — Part 2

In Part 2 of this series we will look at some of the circuits used in this high-performance transceiver.

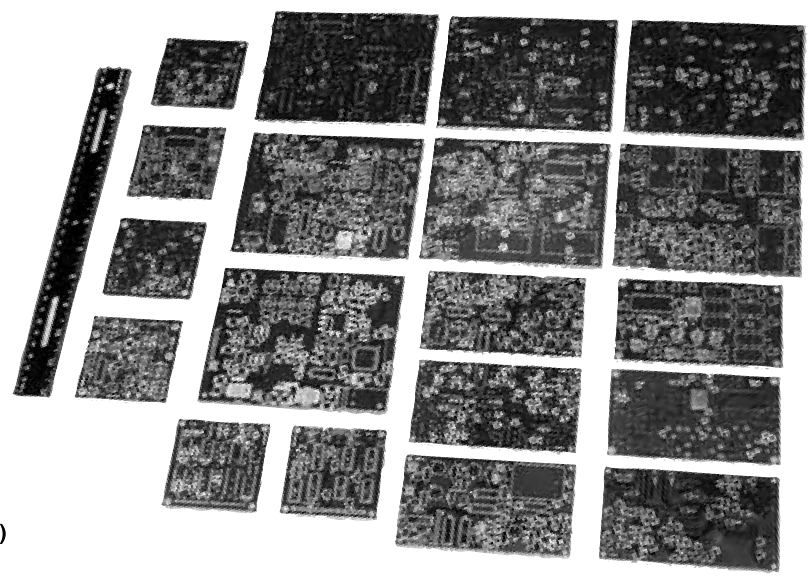


Visible from the left are the FSYNTH assembly (left side panel), the IF75BC assembly (top left), the automatically switched half-octave receiver band-pass and transmitter high power, low-pass filter bank assembly, and the DFCB command and control assembly and keypad mounted on the back of the front panel. Front panel, side panels, top and bottom are removable allowing access to the assemblies.

Mission — The *Star-10* transceiver has been a unique research experience into understanding what can be done from the laws-of-physics point of view in receiver and transceiver dynamic range performance. This research has been performed over a period of five years with parts, technologies and packaging means available to me at the time. The transceiver has been implemented with some unique parts that may no longer be available. The *Star-10* development has been a purely scientific endeavor intended primarily to understand what could be done to achieve ultimate receiver performance. Although the results have been outstanding, slightly better results may be possible using newer technologies and parts. The *Star-10* project was not intended as a commercial product. Its duplication is probably not economically feasible.

Introduction

In Part 1 of this series, I presented a system design criteria for a modern double conversion transceiver, namely the *Star-10*. The primary goal of this design was to produce a continuous HF coverage system with consistent high dynamic range receiver performance over the entire frequency range of 1.8 MHz to 30 MHz. I wanted to build a radio that rivals the performance of today's top-of-the-line equipment. The focus was how to design a no-compromise broadband radio, obtaining superior performance without resorting to a channelized, amateur-band-only design. The accent was put on good image and spurious rejection, using an up convert/down convert design, ample



(A)

(B)

Figure 6 — Part A shows the double-sided, plated-through-hole PC boards developed for the *Star-10* transceiver ready for assembly. Part B shows several of the completed assemblies for the *Star-10* transceiver. Starting from top left, PDAF (product detector/audio); IF9RX (receiver second IF); IF9TX (transmitter first IF); PLXO / MRU (phase locked crystal oscillator / master reference unit); IF75BC (bilateral front end converter), and FSYNTH / FRU (frequency synthesizer / frequency reference unit). For functionality of these blocks, refer to Figure 2 in Part 1 of the article, in the Nov/Dec 2007 issue of *QEX*.

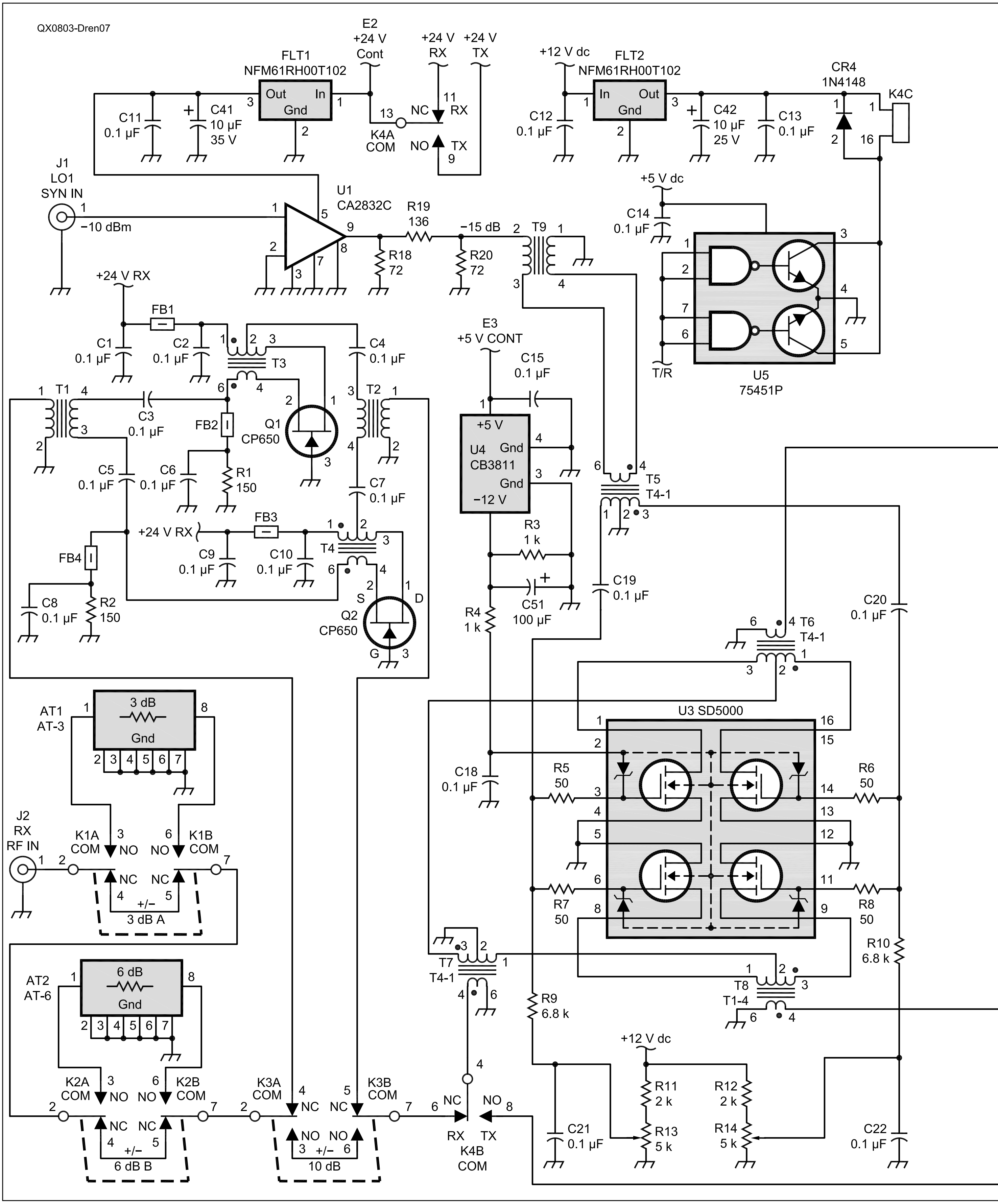
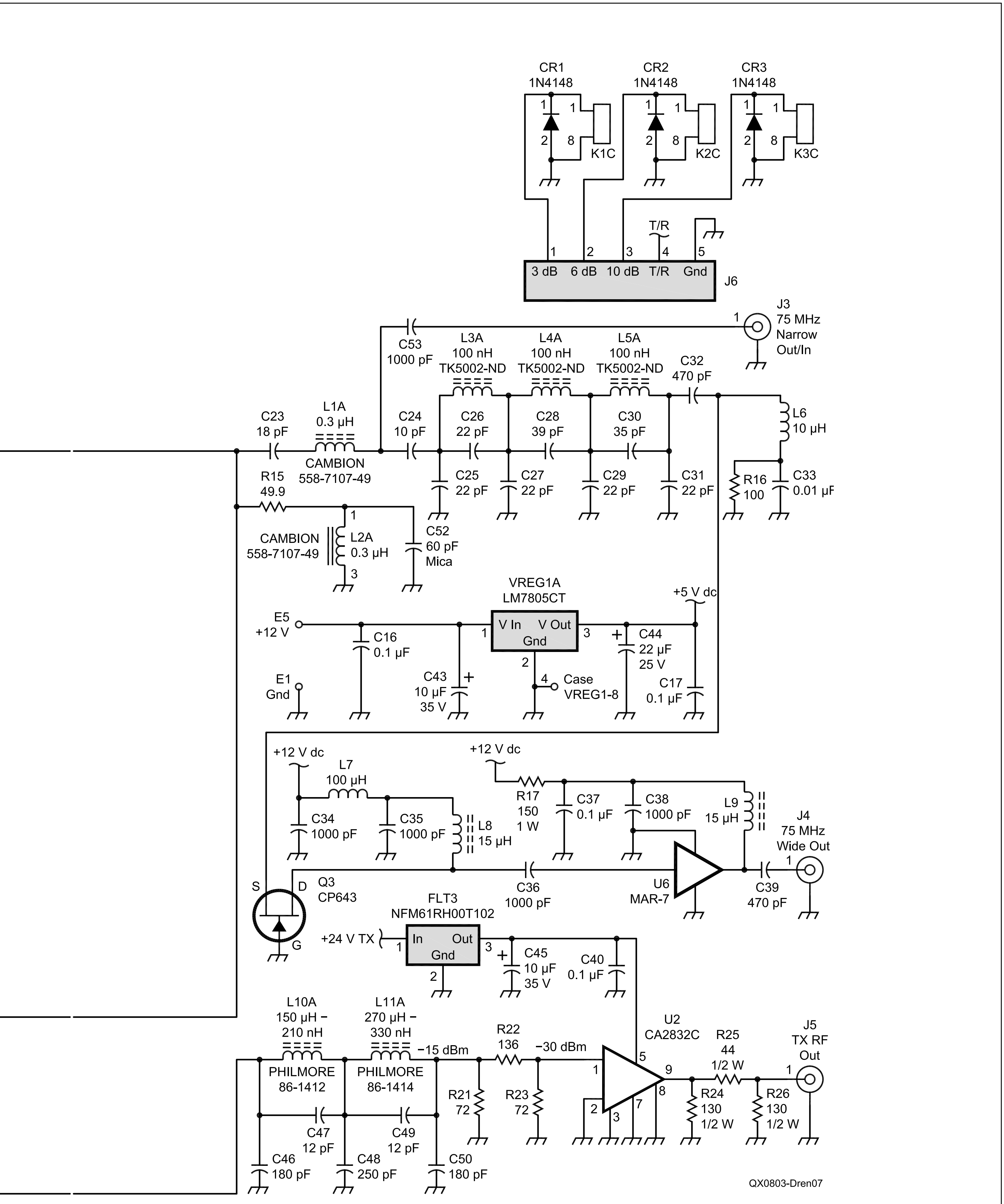


Figure 7 — Schematic diagram of the front end bilateral converter assembly, IF75BC.


CR1
1N4148
CR2
1N4148
CR3
1N4148
K1C
K2C
K3C
T/R
3 dB 6 dB 10 dB T/R Gnd
J6
J3
75 MHz
Narrow
Out/In
C53
1000 pF
L3A
100 nH
TK5002-ND
L4A
100 nH
TK5002-ND
L5A
100 nH
TK5002-ND
C32
470 pF
L6
10 µH
C23
18 pF
L1A
0.3 µH
CAMBION
558-7107-49
C24
10 pF
C26
22 pF
C28
39 pF
C30
35 pF
C25
22 pF
C27
22 pF
C29
22 pF
C31
22 pF
R16
100
C33
0.01 µF
R15
49.9
CAMBION
558-7107-49
L2A
0.3 µH
C52
60 pF
Mica
VREG1A
LM7805CT
+5 V dc
E5
+12 V
V In V Out
Gnd
C16
0.1 µF
C44
22 µF
25 V
E1
Gnd
C43
10 µF
35 V
Case
VREG1-8
C17
0.1 µF
+12 V dc
L7
100 µH
+12 V dc
R17
150
1 W
C37
0.1 µF
C38
1000 pF
L9
15 µH
C34
1000 pF
C35
1000 pF
L8
15 µH
J4
75 MHz
Wide Out
Q3
CP643
C36
1000 pF
U6
MAR-7
C39
470 pF
FLT3
NFM61RH00T102
+24 V TX
In Out
Gnd
C45
10 µF
35 V
C40
0.1 µF
L10A
150 µH –
210 nH
L11A
270 µH –
330 nH
U2
CA2832C
R25
44
1/2 W
J5
TX RF
Out
PHILMORE
86-1412
PHILMORE
86-1414
–15 dBm
R22
136
–30 dBm
R21
72
R23
72
R24
130
1/2 W
R26
130
1/2 W
C47
12 pF
C49
12 pF
C46
180 pF
C48
250 pF
C50
180 pF
QX0803-Dren07

automatically switched front end and IF filtering. The radio uses a DDS-Driven PLL synthesizer. Thus, the *Star-10* design resulted in a 75 MHz first IF and a 9 MHz second IF architecture, using a novel bilateral concept, a complex array of old and new technologies, circuits and packaging techniques. After ample system analysis, intense circuit design, multiple brass boarding and testing, PC board layouts were developed and four sets of boards were manufactured, populated and tested again and again before the final implementation. Two transceivers were developed using these boards, a work-in-progress prototype by KG6NK, and the featured *Star-10* model presented here.

The unpopulated double-sided, plated-through PC boards developed specifically for the *Star-10* transceiver are shown in Figure 6A. Some of the completed and tested assemblies are shown in Figure 6B. [To provide easy reference between the parts of this series, we have numbered the Figures consecutively throughout. — *Ed.*]

I will next discuss the major assemblies and major design details of the *Star-10* transceiver. For clarity, you should first read Part 1 of this series in order to better understand the functionality of each of the assemblies. Part 1 is available on the ARRL *QEX* Web site at **www.arrl.org/qex**. You will be constantly directed to the transceiver's block diagram in Figure 2 from Part 1 to better understand where a specific assembly fits. To make the best use of printed space, only major blocks will be discussed in detail. As previously indicated, no circuit layouts, construction plans or software listings are offered in this article series.

Front End (IF75BC)

As the name implies, this is the first IF (75 MHz) or the bilateral 75 MHz converter. This assembly is a key ingredient of the *Star-10* receiver design because it sets the entire system noise figure and intercept point. IF75BC operates in receive as well as transmit modes.

Referring to Figure 2 from Part 1, the IF75BC assembly provides receiver up conversion for the entire HF range from 1.8 MHz to 30 MHz, to the 75 MHz IF, or down conversion from this IF to the same HF range of 1.8 MHz to 30 MHz in transmit. The IF75BC is preceded by a half-octave band-pass filter bank (composed of eight automatically selectable filters) in receive, the power linear amplifier and a similar half-octave low-pass, high power filter bank (composed of eight automatically selectable equivalent filters) in transmit. To keep intermodulation distortion under control, no PIN switching diodes are used to select filters. All filters in the *Star-10* are switched with either miniature Teledyne RF relays, or high power RF relays. These assemblies will be discussed in more detail later. A schematic diagram of IF 75BC is shown in Figure 7. The actual IF75BC board and assembly implementation are shown in Figure 8.

The 75 MHz first IF choice puts the receiver image away by 150 MHz at any frequency between 1.8 MHz and 30 MHz. This works in direct conjunction with the proper

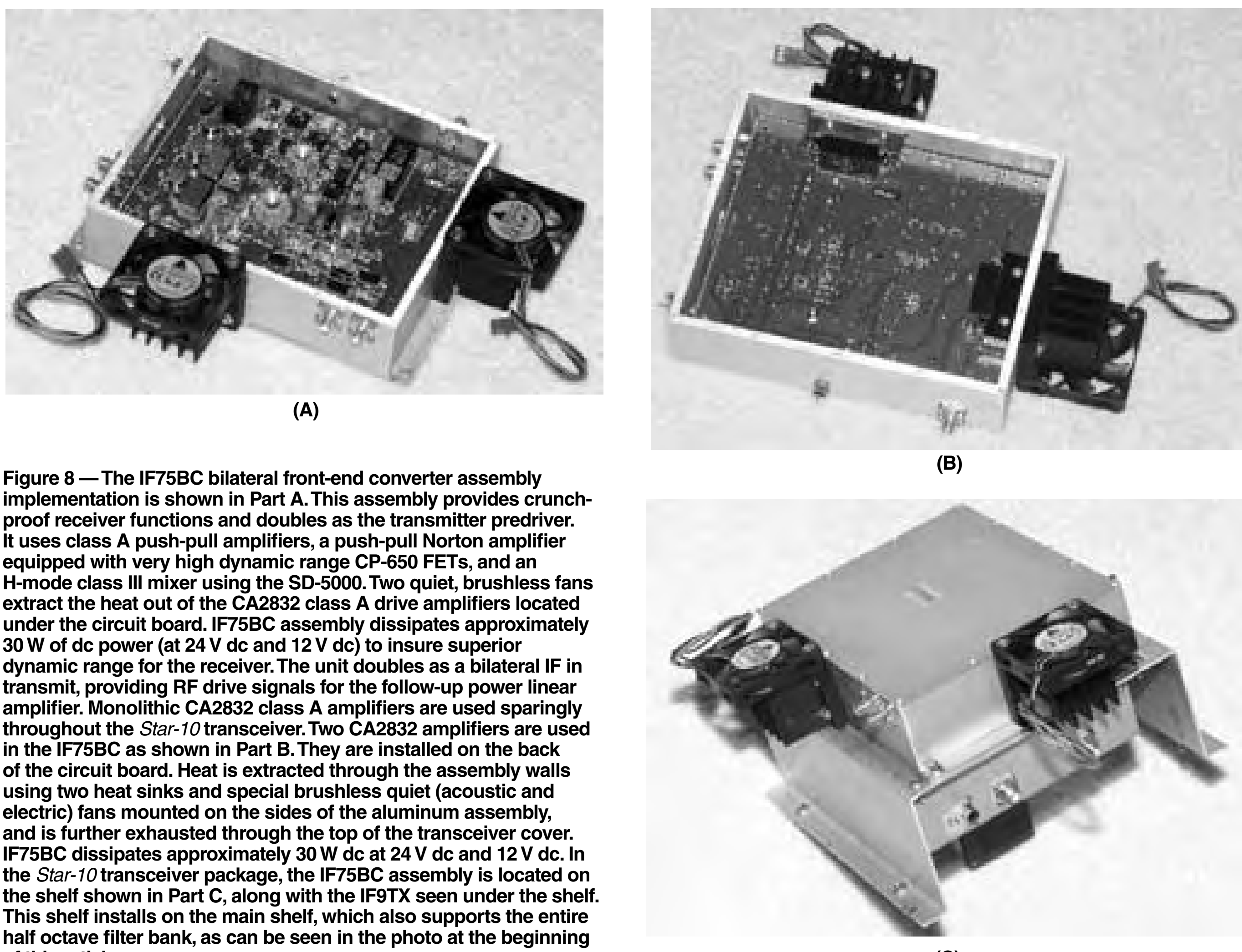


Figure 8 — The IF75BC bilateral front-end converter assembly implementation is shown in Part A. This assembly provides crunch-proof receiver functions and doubles as the transmitter predriver. It uses class A push-pull amplifiers, a push-pull Norton amplifier equipped with very high dynamic range CP-650 FETs, and an H-mode class III mixer using the SD-5000. Two quiet, brushless fans extract the heat out of the CA2832 class A drive amplifiers located under the circuit board. IF75BC assembly dissipates approximately 30 W of dc power (at 24 V dc and 12 V dc) to insure superior dynamic range for the receiver. The unit doubles as a bilateral IF in transmit, providing RF drive signals for the follow-up power linear amplifier. Monolithic CA2832 class A amplifiers are used sparingly throughout the *Star-10* transceiver. Two CA2832 amplifiers are used in the IF75BC as shown in Part B. They are installed on the back of the circuit board. Heat is extracted through the assembly walls using two heat sinks and special brushless quiet (acoustic and electric) fans mounted on the sides of the aluminum assembly, and is further exhausted through the top of the transceiver cover. IF75BC dissipates approximately 30 W dc at 24 V dc and 12 V dc. In the *Star-10* transceiver package, the IF75BC assembly is located on the shelf shown in Part C, along with the IF9TX seen under the shelf. This shelf installs on the main shelf, which also supports the entire half octave filter bank, as can be seen in the photo at the beginning of this article.

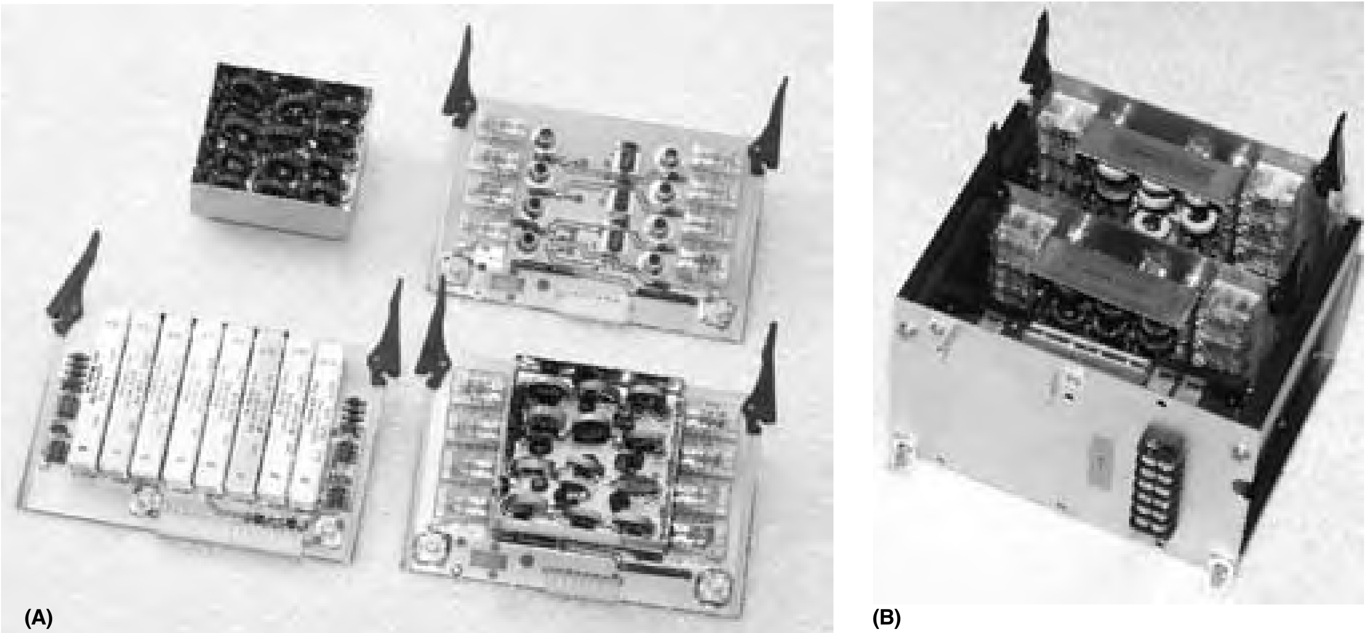


Figure 9 — Part A shows receiver and transmitter half-octave filters banks. Automatically switched half-octave filter banks are shown in Part B, where the motherboard/cage assembly holds the receiver front-end filter boards (eight filters) as well as the transmitter high-power, low-pass filter boards (eight filters). This assembly is located on a shelf shown on the right side of the transceiver, as shown in the lead photo. The DFCB command and control assembly automatically selects the filters.

half-octave filter being selected in the front-end banks. The amount of rejection provided is consequently uniform throughout the coverage due to the proper selection of the half-octave ranges. (See References 1, 2, 3, listed at the end of this article.) A high-pass receiver front end filter, which is sometimes used in general coverage designs, was found unnecessary due to the extremely good shape factor offered by the half-octave band-pass filters. Conversely, the proper half-octave low-pass filter selected in the transmit chain ensures equally good spurious and harmonic rejection throughout the entire frequency range.

Looking at the schematic diagram in Figure 7, the filtered received RF signals from the half-octave band-pass filter bank enter the receiver circuits of the IF75BC board assembly at J2 through the advanced intercept point attenuator (AIPA) and the +10 dB push-pull preamplifier located on this board. This combination allows for the programmable AIPA attenuators (part of the gain control system) to be inserted in the receiver front end if so desired. Because of the dynamic range capability of the *Star-10*, these functions have not been used extensively since good results were obtained with the preamplifier on and no attenuators.

Three front panel programmable attenuation steps are provided by AIPA: 3 dB, 6 dB and 10 dB. Commands for these selections enter the IF75BC through the J6 connector. The 3 dB and 6 dB positions are imple-

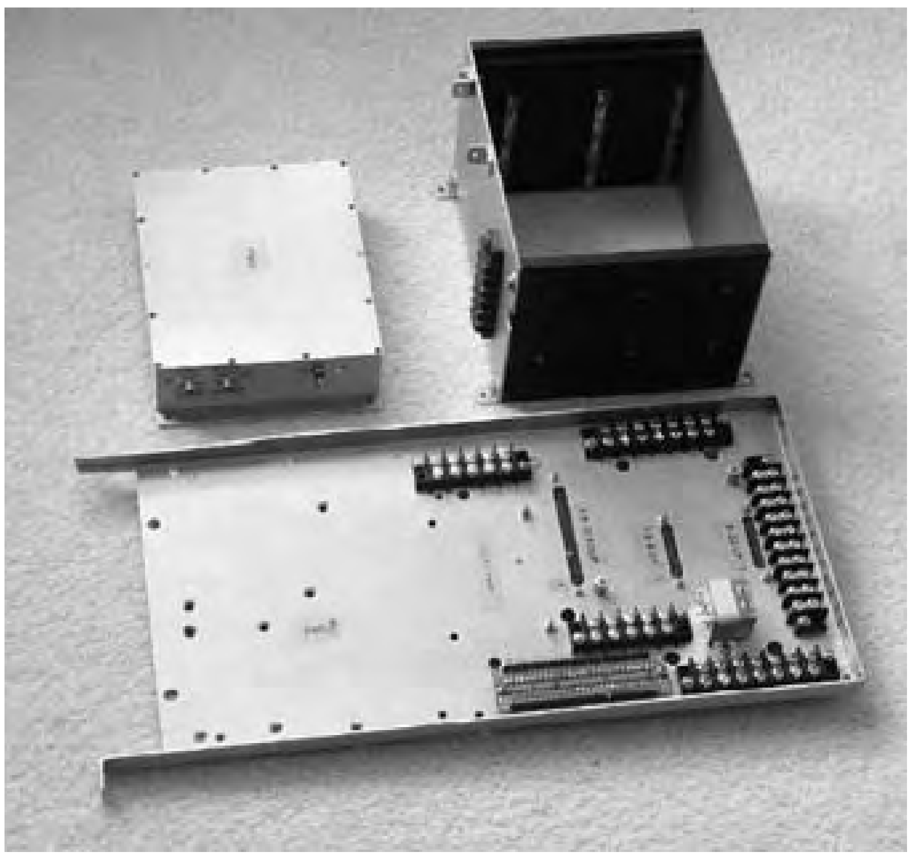


Figure 10 — View of the bottom shelf (motherboard), which holds the automatically switched half-octave filter banks and the motherboard cage (at the top right corner of the photo). Command and control lines have been wired to the connectors visible in the slots in the shelf.

mented by inserting a 3 dB or a 6 dB pad via corresponding relays (AT1, K1 and AT2, K2) in the circuit, while the 10 dB function is implemented through totally bypassing the push-pull amplifier, using K3 as shown. The preamp can always be on because of the dynamic range capability of the *Star-10*. The AIPA functions are remote controlled from the front panel via miniature RF relays located on the IF75BC board. The front panel switch (marked AIPA) that controls these attenuators also controls three LED indicators showing what is selected on the composite front panel display (dial) as shown in the lead photo.

To ensure the high dynamic range for the receiver, IF75BC uses an adaptation of a push-pull Norton amplifier, using very high dynamic range CP-650 FETs. This preamplifier, as well as other IF75BC functions, use 24 V dc in addition to 12 V dc and other voltages. The power consumption of the IF75BC front end board and assembly is around 30 W dc, requiring heat sinks as shown in Figure 8 A, B and C.

The Norton amplifier circuit was initially developed and patented by David Norton and Allen Podell in 1975 (reference 4, 5, 6). This circuit constitutes a novel development in the application of negative feedback techniques to active double-balanced mixers, in which the concept of single-transformer "loss less feedback" is employed to improve both, the intercept point and the noise figure. The Norton design uses transformer coupling to achieve "noiseless negative feedback" – a truly outstanding approach.

Loss less feedback amplifiers have been recognized as an outstanding means of providing high dynamic range, in terms of both linearity and noise figure. In the following years since its invention, various forms of the Norton amplifier have found wide usage in good communications receivers and radio astronomy applications.

A variation on the Norton amplifier was further described by Joe Reisert in *ham radio* magazine (reference 7). The circuit has been further improved by Jacob Makhinson and was described in detail in references 8, 9, 10, 11, 12.

Looking at Figure 7, the conditioned RF signals from AIPA enter the first mixer U3 which is used in an H-mode (references 6, 7, 8, 9) biasing system. The variable high resolution LO signal from the synthesizer (FRU - FSYNTH) is presented to the mixer via J1 and U1, via a CA2832 class A monolithic amplifier (note: *Star-10* makes ample use of the Motorola CA2832 monolithic amplifiers) operating at 24 V. Thus, the LO level is built up from approximately -9 dBm to about +27 dBm. Mixer biasing is further provided through R13, R14 and U4. The H-mode mixer used is typical of the design described in the above references. However, most of these designs have been used in low IF configurations (e.g. 9 MHz) and with limited RF/LO bandwidths. They are usually fed by out of phase digital drivers which maintain tight LO jitter and phase coherence over relatively narrow frequency ranges. However, using such designs over very broad

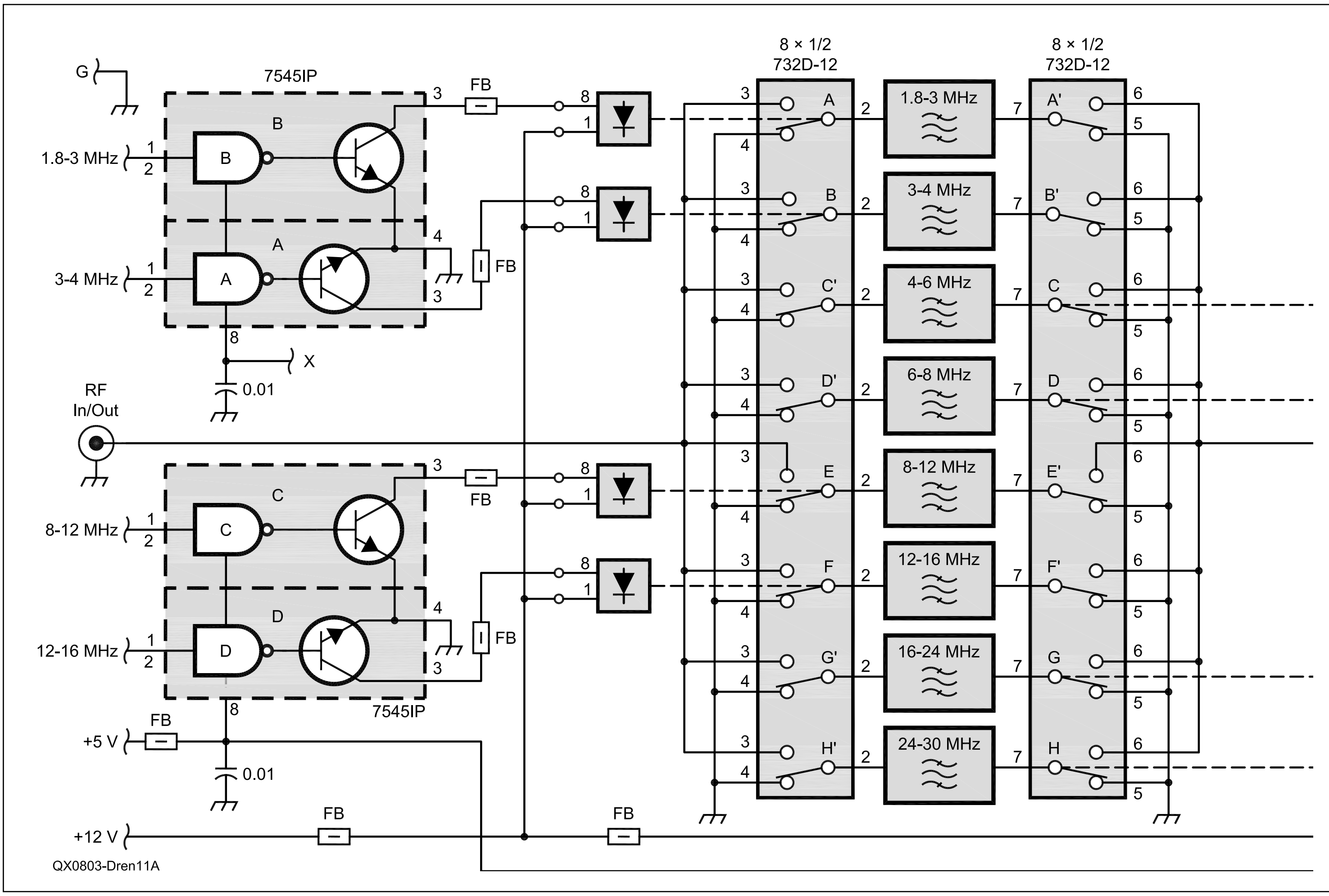


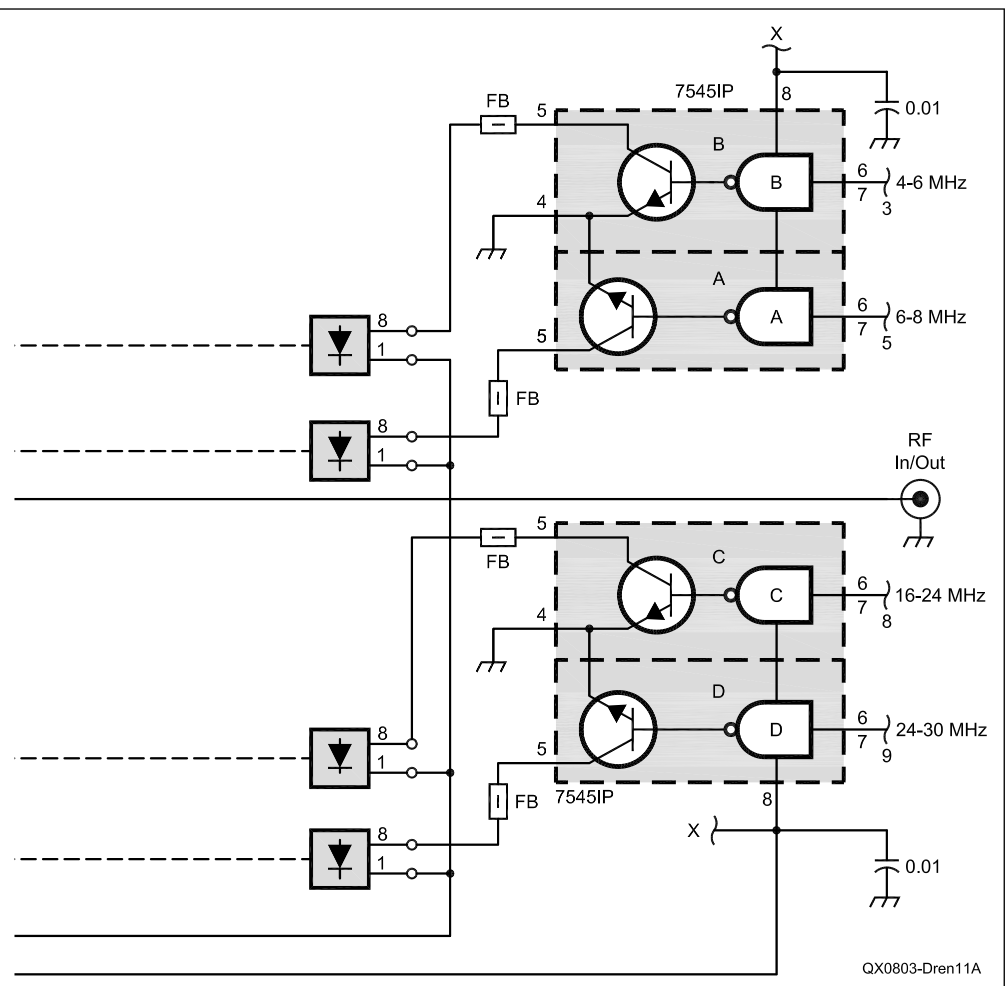
Figure 11A — The schematic diagram for the receiver band-pass filter bank.

frequency ranges such as the four octaves used in the *Star-10* would require sub - pico second rise time phase matching between the digital drivers. Because of the *Star-10* broadband nature, it was found impractical to provide LO drive via digital means. After long analysis and experimentation, it was found that using a transformer combination can provide the required phase balance over the entire frequency coverage with minor phase mismatching consequences. Following intense testing, this solution was found to be a practical compromise.

Making the preamplifier and the H-mode mixer work in the actual IF75BC board required ample circuit layout planning, where connecting paths in the double sided plated through PC board was implemented with short and balanced paths, which were trimmed equally to promote amplifier stability. Additional ferrite beads were used together with short leads to prevent oscillation. The negative biasing supply for the SD-5000 mixer was achieved using a dc-to-dc converter at U4 as shown. Considerable care was taken in the entire board design to ensure proper ground distribution and avoid resonant features.

The transmit chain on IF75BC, when activated via the T/R relay K4, outputs RF signals to the power linear amplifier through the 30 MHz low-pass filter made of L10, L11, C46 through C50, and another class A - CA2832 monolithic amplifier, U2. Driver circuits for the RF relays on IF75BC as well as throughout the entire transceiver use high current open collector digital line drivers 75451 ICs (U5 on this board). The RF output at J5 goes further to the high power linear amplifier, and to the automatically switched half-octave low-pass filter banks, through the RF power transmitter gain control (TGC) circuits and further through the main T/R switch, to the antenna. The T/R relay on IF75BC which is facilitated through the on board K4, also provides proper switched 24 V dc to the bilateral amplifier (BILAT AMP) assembly located further down in the 75 MHz IF chain as shown in Figure 2, Part 1 of this article series.

There are two 75 MHz IF receiver outputs on the IF75BC; the first is diplexed via L2, C52, C53 and is further output at J3 to be input to the quartz crystal roofing filter assembly, FL75. This signal serves in receive as well as in transmit as the narrow 75 MHz IF output/input. The other output at J4 serves as the 75 MHz wide IF (500 kHz) intended for spectrum analysis and noise blanker functions to be achieved further in IF9NB. This wide band signal follows the path from C24 through the 500 kHz band pass filter made of L3 through L5 and C25 through C32 and further through Q3 and U6. This completes the IF75BC assembly description.



Receiver and Transmitter Half-Octave Filter Banks

Looking at the *Star-10* transceiver block diagram from Figure 2 of Part 1, the IF75BC assembly is preceded by the half-octave band-pass and low-pass filters banks as shown in Figure 9. The actual location of this assembly in the *Star-10* transceiver package can be seen on the right side of the leading photo at the beginning of this Part.

The design of these filters and their functionality in a general coverage HF transceiver or receiver has been previously described in great detail in references 1, 2 and 3. The *Star-10* transceiver uses this design in a new mechanical implementation specific to this transceiver package.

There are eight automatically selectable band-pass receiver filters (bottom left board of Figure 9 A) and eight high-power low-pass similar filters (the remaining assemblies shown in Figure 9 A). The filter banks are plug in shielded assemblies as shown. They insert into the PC boards that contain the control circuits utilizing 75451 line drivers to switch corresponding RF relays, which in turn use commands from the DFCB assembly microprocessor to select the proper receive and transmit combination. The boards equipped with the plug in filter banks (as shown) are in turn, plug-in assemblies themselves. They insert into a machined motherboard cage assembly as shown in Figure 9 B. Command signals coming from DFCB board and RF connectors are provided at the bottom of the assembly which is supported by the bottom shelf of the *Star-10* system as shown in Figure 10.

The schematic diagram for the receiver's band-pass filters - bank is shown in Figure 11 A. The schematic diagram for the high power low-pass filters banks (two assemblies) is shown in Figure 11 B. There are eight band-pass filters in the receiver assembly and four low-pass filters in each of the two low-pass assemblies, for a total of eight equivalent

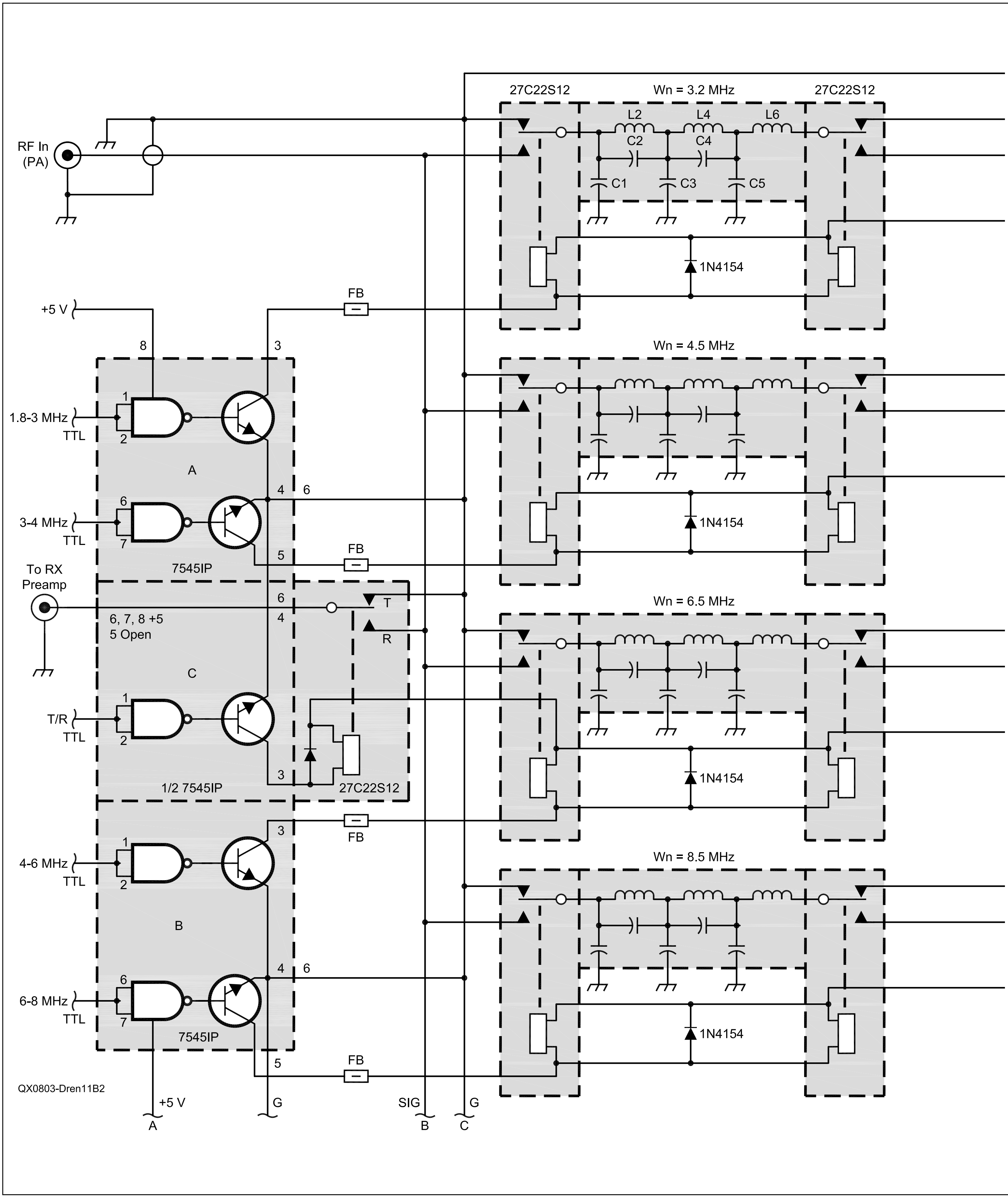
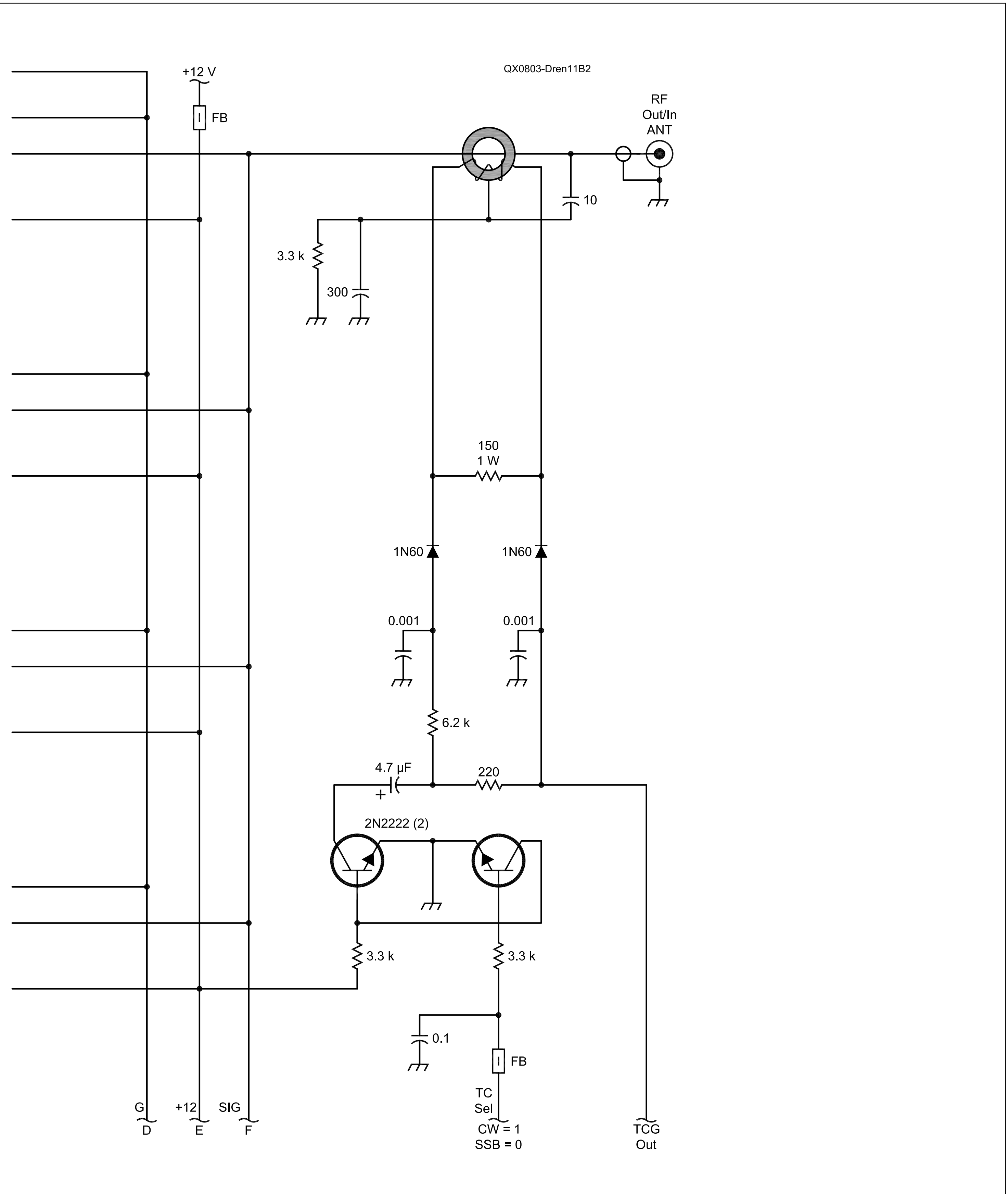


Figure 11B — The schematic diagram for the high-power, low-pass filter banks.


QX0803-Dren11B2
+12 V
FB
RF
Out/In
ANT
10
3.3 k
300
150
1 W
1N60
1N60
0.001
0.001
6.2 k
4.7 µF
220
2N2222 (2)
3.3 k
3.3 k
0.1
FB
G
D
+12
E
SIG
F
TC
Sel
CW = 1
SSB = 0
TCG
Out

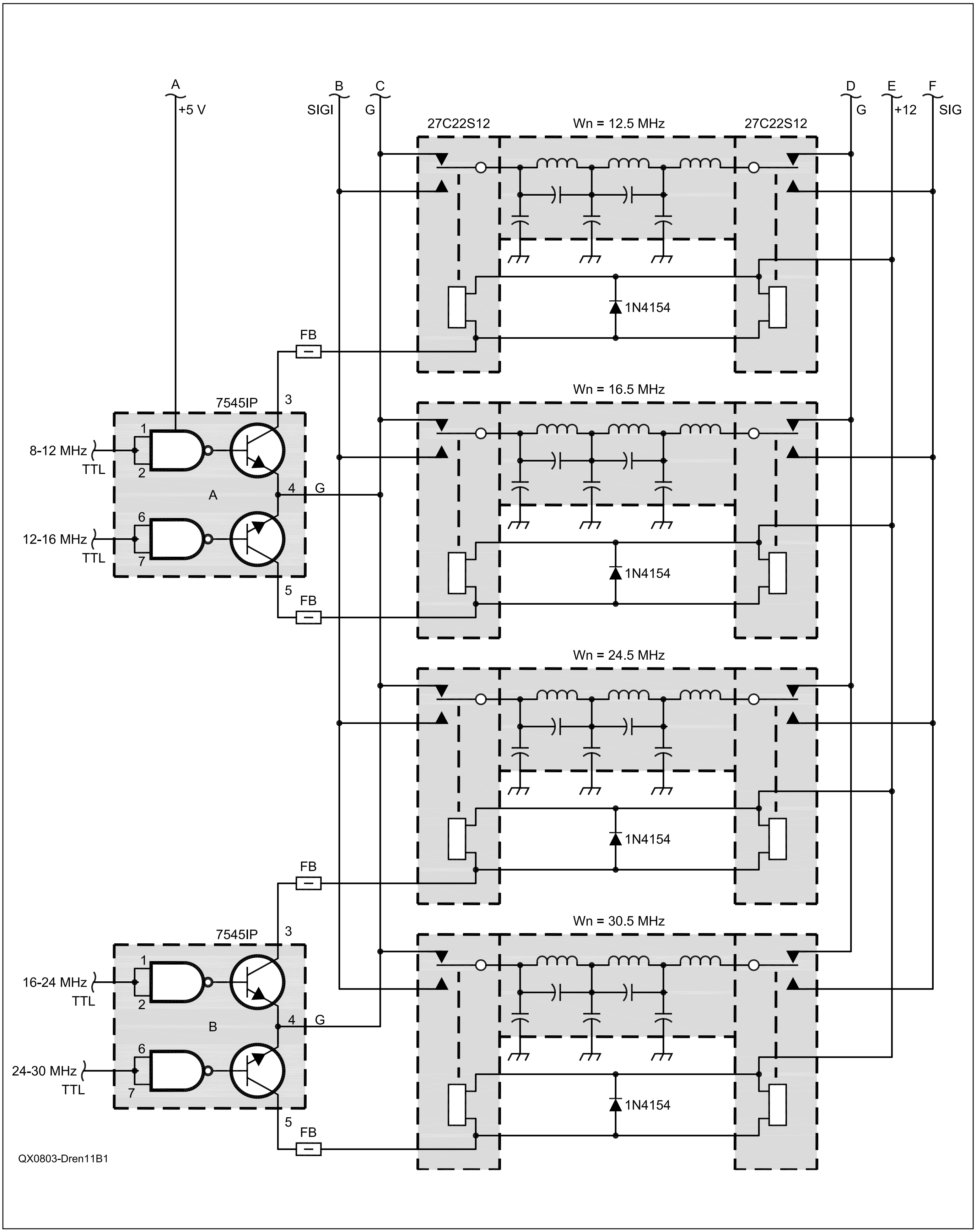


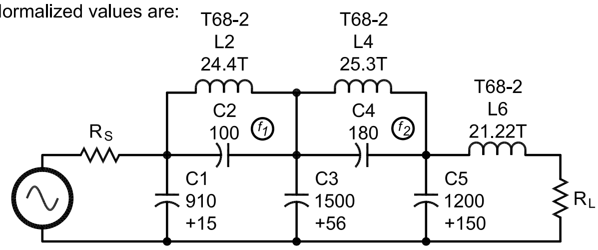
Figure 11B continued

QX0803-Dren11C

#1

f_C = 3.2 MHz Band = 1.8 − 3 MHz
Reject 6 MHz by 60 dB
f_C : Reject = 1.875:1

Use A C0615C θ = 35° Filter
Minimum Attenuation At 6 MHz = 67.8 dB
Normalized values are:



R_S = 1
C_1 = 0.9316
L_2 = 1.368
C_4 = 0.1880
C_5 = 1.371

R_L = 1
C_2 = 0.1082
C_2 = 1.564
L_4 = 0.1466
L_6 = 1.033

f_1 = 2.5989
f_2 = 1.9051

the denormalized values are:

R_S = 50
C_1 = 926.7* pF (910 + 15)**
L_2 = 3.40 µH
C_4 = 187 pF (180)
C_5 = 13.64 pF (1200 + 150)

R_L = 50
C_2 = 107.6 pF (100)
C_3 = 1556 pF (1500 + 56)
L_4 = 3.65 µH
L_6 = 2.568 µH

f_1 = 8.316 MHz
f_2 = 6.0963 MHz

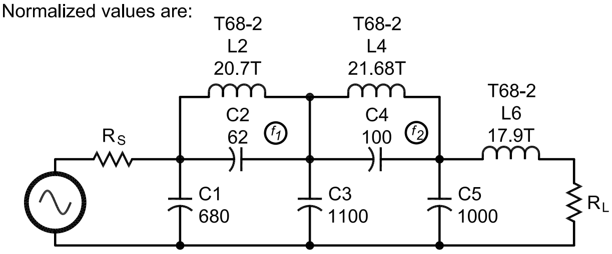
tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

* Design value
** Actual value used

#2

f_C = 4.5 MHz Band = 3 − 4 MHz
Reject 9 MHz
f_C : Reject ratio = 2:1

Use A C0615C θ = 32° Filter
Minimum Attenuation At 9 MHz = 72.8 dB
Normalized values are:



R_S = 1
C_1 = 0.9492
L_2 = 1.393
C_4 = 0.1540
C_5 = 1.395

R_L = 1
C_2 = 0.08912
C_3 = 1.601
L_4 = 1.518
L_6 = 1.034

f_1 = 2.8385
f_2 = 2.06813

the denormalized values are:

R_S = 50
C_1 = 671.4 pF (680)
L_2 = 2.46 µH
C_4 = 108.9 pF (100)
C_5 = 986.7 pF (1000)

R_L = 50
C_2 = 63 pF (62)
C_3 = 1132.4 pF (1100)
L_4 = 2.68 µH
L_6 = 1.83 µH

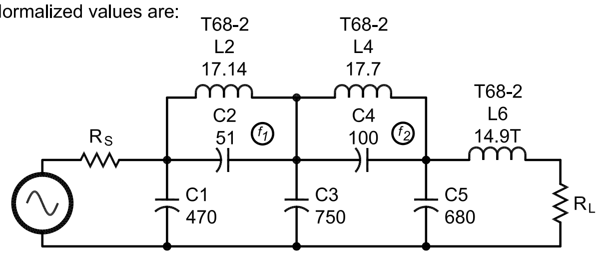
f_1 = 12.773 MHz
f_2 = 9.3066 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

#3

f_C = 6.5 MHz Band = 4 − 6 MHz
Reject 12 MHz
f_C : Reject = 1.846:1

Use A C0615C θ = 35° Filter
Minimum Attenuation At 12 MHz = 67.8 dB
Normalized values are:



R_S = 1
C_1 = 0.9316
L_2 = 1.368
C_4 = 0.1880
C_5 = 1.371

R_L = 1
C_2 = 0.1082
C_2 = 1.564
L_4 = .1.466
L_6 = 1.033

f_1 = 2.59897
f_2 = 1.9051

the denormalized values are:

R_S = 50
C_1 = 456.2 pF (470)
L_2 = 1.675 µH
C_4 = 92 pF (100)
C_5 = 671.4 pF (680)

R_L = 50
C_2 = 53 pF (51)
C_3 = 766 pF (750)
L_4 = 1.79 µH
L_6 = 1.265 µH

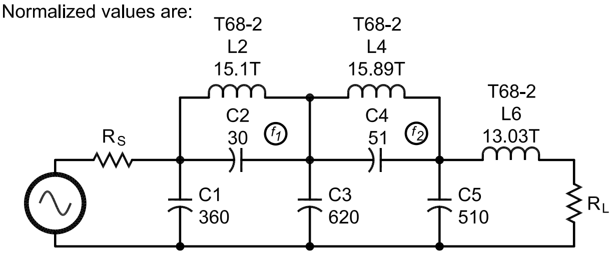
f_1 = 16.893 MHz
f_2 = 12.383 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

#4

f_C =8.5 MHz Band = 6 − 8 MHz
Reject 18 MHz
f_C : Reject = 2.11:1

Use A C0615C θ = 31° Filter
Minimum Attenuation At 18 MHz = 74.5 dB
Normalized values are:



R_S = 1
C_1 = 0.9547
L_2 = 1.400
C_4 = 0.1436
C_5 = 1.402

R_L = 1
C_2 = 0.08325
C_2 = 1.612
L_4 = 1.535
L_6 = 1.034

f_1 = 2.9287
f_2 = 2.1298

the denormalized values are:

R_S = 50
C_1 = 357.5 pF (360)
L_2 = 1.31 µH
C_4 = 53.8 pF (50)
C_5 = 525 pF (510)

R_L = 50
C_2 = 31.2 pF (30)
C_3 = 603.7 pF (620)
L_4 = 1.44 µH
L_6 = 0.968 µH

f_1 = 24.894 MHz
f_2 = 18.1033 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

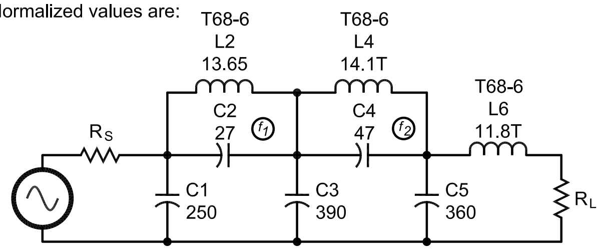
Figure 11C — Design values for the low-pass filter banks. The band-pass design is directly derived from the low-pass design.

#5

QX0803-Dren11C

f_C = 12.5 MHz Band = 8 − 12 MHz
Reject 24 MHz
f_C : Reject = 1.92:1

Use A C0615C θ = 34° Filter
Minimum Attenuation At 24 MHz = 69.4 dB
Normalized values are:



R_S = 1	R_L = 1
C_1 = 0.9377	C_2 = 0.101
L_2 = 1.376	C_2 = 1.577
C_4 = 0.1761	L_4 = 1.484
C_5 = 1.379	L_6 = 1.034
f_1 = 2.6741	f_2 = 1.9561

the denormalized values are:

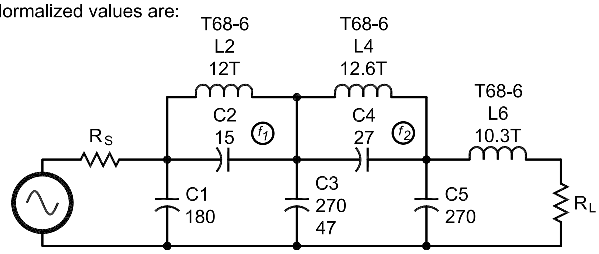
R_S = 50	R_L = 50
C_1 = 238.8 pF (250)	C_2 = 25.9 pF (27)
L_2 = 0.876 µH	C_3 = 401.6 pF (390)
C_4 = 44.8 pF (47)	L_4 = 0.945 µH
C_5 = 351.1 pF (360)	L_6 = 0.658 µH
f_1 = 33.426 MHz	f_2 = 24.451 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

#6

f_C = 16.5 MHz Band = 12 − 16 MHz
Reject 36 MHz
f_C : Reject ratio = 2.18:1

Use A C0615C θ = 30° Filter
Minimum Attenuation At 36 MHz = 76.3 dB
Normalized values are:



R_S = 1	R_L = 1
C_1 = 0.96	C_2 = 0.0776
L_2 = 1.408	C_3 = 1.623
C_4 = 0.1337	L_4 = 1.551
C_5 = 1.410	L_6 = 1.034
f_1 = 3.02499	f_2 = 2.19586

the denormalized values are:

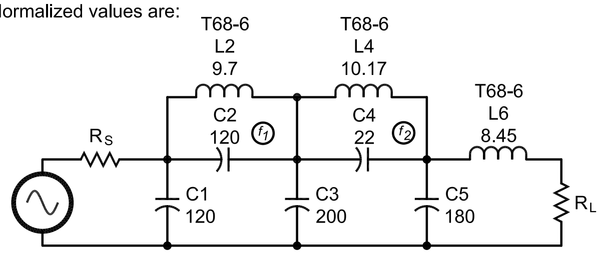
R_S = 50	R_L = 50
C_1 = 185.19 pF (180)	C_2 = 14.9 pF (15)
L_2 = 0.679 µH	C_3 = 313.1 pF (270 + 47)
C_4 = 25.8 pF (27)	L_4 = 0.748 µH
C_5 = 272 pF (270)	L_6 = 0.4987 µH
f_1 = 49.9123 MHz	f_2 = 36.2317 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

#7

f_C = 24.5 MHz Band = 16 − 24 MHz
Reject 48 MHz
f_C : Reject = 1.96:1

Use A C0615C θ = 33° Filter
Minimum Attenuation At 48 MHz = 71.1 dB
Normalized values are:



R_S = 1	R_L = 1
C_1 = 0.9436	C_2 = 0.09523
L_2 = 1.385	C_2 = 1.589
C_4 = 0.1648	L_4 = 1.501
C_5 = 1.387	L_6 = 1.034
f_1 = 2.75377	f_2 = 2.0103

the denormalized values are:

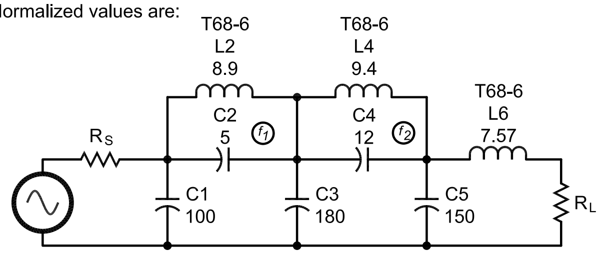
R_S = 50	R_L = 50
C_1 = 122.6 pF (120)	C_2 = 12.37 pF (12)
L_2 = 0.449 µH	C_3 = 206.4 pF (200)
C_4 = 21.4 pF (22)	L_4 = 0.487 µH
C_5 = 180.2 pF (180)	L_6 = 0.336 µH
f_1 = 67.467 MHz	f_2 = 49.292 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

#8

f_C = 30.5 MHz Band = 24 − 30 MHz
Reject 72 MHz
f_C : Reject = 2.36:1

Use A C0615C θ = 27° Filter
Minimum Attenuation At 72 MHz = 82 dB
Normalized values are:



R_S = 1	R_L = 1
C_1 = 0.9747	C_2 = 0.06212
L_2 = 1.429	C_2 = 1.654
C_4 = 0.1066	L_4 = 1.595
C_5 = 1.430	L_6 = 1.035
f_1 = 3.3568	f_2 = 2.4244

the denormalized values are:

R_S = 50	R_L = 50
C_1 = 101.7 pF (100)	C_2 = 6.5 pF (5)
L_2 = 0.373 µH	C_3 = 172.6 pF (180)
C_4 = 11.1 pF (12)	L_4 = 0.416 µH
C_5 = 149.2 pF (150)	L_6 = 0.270 µH
f_1 = 102.38 MHz	f_2 = 73.944 MHz

tune L_2 , C_2 for an attenuation peak at f_1
tune L_4 , C_4 for an attenuation peak at f_2

half-octave filters (1.8 to 3, 3 to 4, 4 to 6, 6 to 8, 8 to 12, 12 to 16, 16 to 24, and 24 to 30 MHz). The chosen electrical design for all filters is the Cauer (elliptical) approach. This type of filter has an in-band characteristic similar to that of a Chebyshev filter; it also has a more abrupt transition band characteristic than the monotonically increasing attenuation of the Chebyshev approach. This design was chosen because of the superior rejection and the relatively easier execution and tuning procedures required. Shown in Figure 11 C are the electrical schematics and design values for all the low-pass filter banks. The band-pass design was directly derived from the low-pass implementation. For a much more in depth discussion on the actual design of these filters, you are directed to my article series from references 1 and 2, which is available on my Web site listed at the end of this article.

75 MHz Bilateral IF

The roofing filter assemblies (FL75), the 75 MHz Bilateral Amplifier (BILAT AMP), and the 75 MHz to 9 MHz Bilateral Converter (IF9BC) will be described together because they constitute the 75 MHz bilateral IF. Looking at the *Star-10* transceiver block diagram from Figure 2 of Part 1, these three assemblies follow the IF75BC providing further signal processing through the 75 MHz bilateral IF (BILAT AMP), and selective signal conditioning through the FL75 roofing filter assembly.

A second conversion to the 9 MHz IF stage (used in receive and transmit) is facilitated through the IF9BC assembly. Physically, the above assemblies are partly located on the left side of the transceiver under the shelf shown in Figure 8 C. The BILAT AMP assembly is located in the center area of the bottom side of the main shelf (for a view of the shelf, see Figure 10) as shown in Figure 12 (the smaller assembly in the center equipped with a fan).

The BILAT AMP and the FL75 roofing filter assemblies are shown in Figure 13. The schematic diagram for the BILAT AMP assembly is shown in Figure 14. The performance characteristics of the bilateral amplifier are shown in Table 1.

Looking at Figure 14, the 75 MHz BILAT AMP uses two back-to-back CA2832 monolithic amplifiers which were discussed earlier. As can be seen, only one of the amplifiers is on at the time, the default being the receiver chain at the top of Figure 14. Power is applied selectively to the respective circuit via the T/R function through the switched 24 V dc lines from IF75BC. In transmit, the power is switched on to the bottom circuit and the top circuit remains dormant for the duration of transmit. Natural isolation between the active circuit and the dormant circuit is provided via the inherent isolation (>20 dB) allowed by the passive splitter/combiner arrangement shown.

One of the 75 MHz IF outputs from IF75BC enters the first section (A) of the roofing filter FL75 (see Figure 2 in Part 1) as shown. Again, all RF interconnects between assemblies in the *Star-10* are 50 ohms, making it easy to use miniature coaxial cables equipped with SMA connectors. The output of the first FL75 filter section is then input to the BILAT AMP at J1, where it enters the first splitter/combiner PSC2-1 (A1) at pin 1 as shown. The receiver path continues at pin 5 of the PSC2-1 and is output to the BIPA circuit located on the IF9BC assembly. The BIPA circuit is a 30 dB –programmable - from the front panel - PIN diode attenuator circuit that will be discussed in more detail later. The return path from the BIPA circuit is input back into the receiver's 75 MHz IF and is further amplified in the BILAT AMP assembly by the CA2832 amplifier at U1, to be recombined with the isolated transmitter path through another PSC2-1 (A2). The output of the BILAT AMP assembly is then output at J2 and is further input to the second section (B) of the FL75 roofing filter assembly. This functionality is true in receive as well as transmit providing true bilateral functionality for the entire 75 MHz IF. It should be noted that the 75 MHz filter assembly has been split in two sections and is intentionally isolated by the amplifier in order to cope with the relatively high IF levels seen at these points in the circuits (see system analysis

Table 1
Bilateral Amplifier (BILAT AMP) Specifications

Mode of operation: Bidirectional OR function (one way active at any given time)
Operating frequency: 75 MHz
Gain (max): +36 dB
NF: 5 dB
1 dB compression point (CP1): +35 dBm
IP3: +50 dBm
RF in (max): +5 dBm
RF out (max) +32 dBm
Vcc: +24 V dc
Ic: 450 mA (one-way active)
Amplification Class: AA

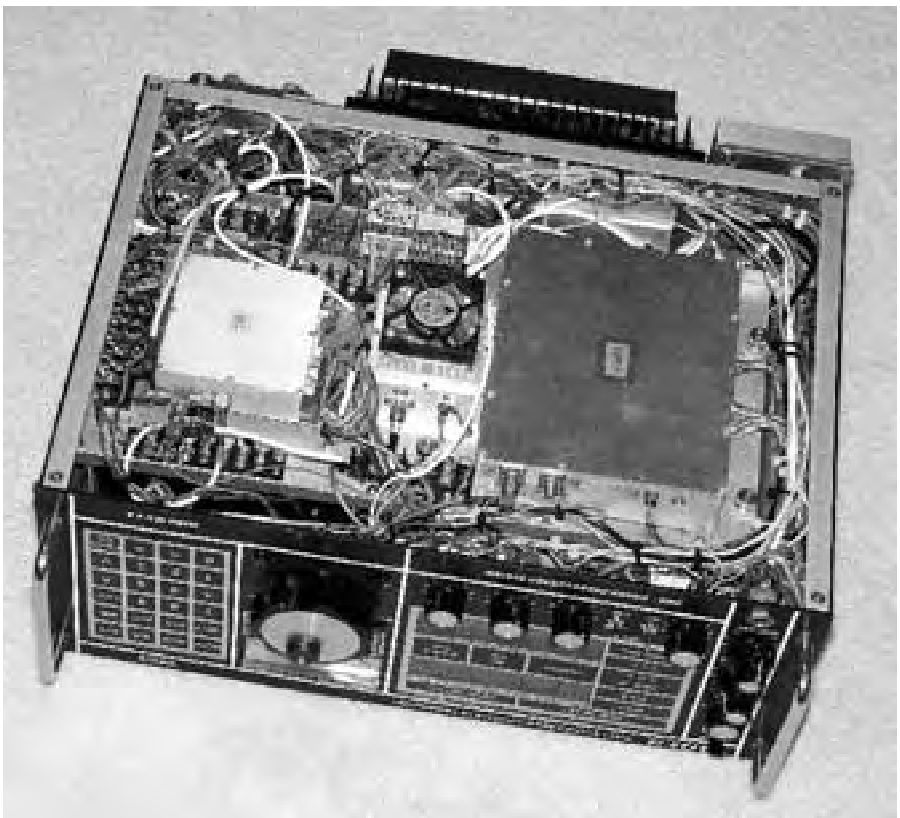


Figure 12 — Bottom view of the *Star-10* transceiver, with the back of the main shelf exposed. Shown in the center is the 75 MHz bilateral amplifier (BILAT AMP) using two back-to-back monolithic CA2832 class A amplifiers (one used in receive and the other in transmit), isolated from each other via splitters/combiners. These high dynamic range amplifiers are capable of 35 dB gain, a 5 dB noise figure and a +50 dBm IP3. Cooling is achieved via another brushless fan extracting the heat through the bottom panel.

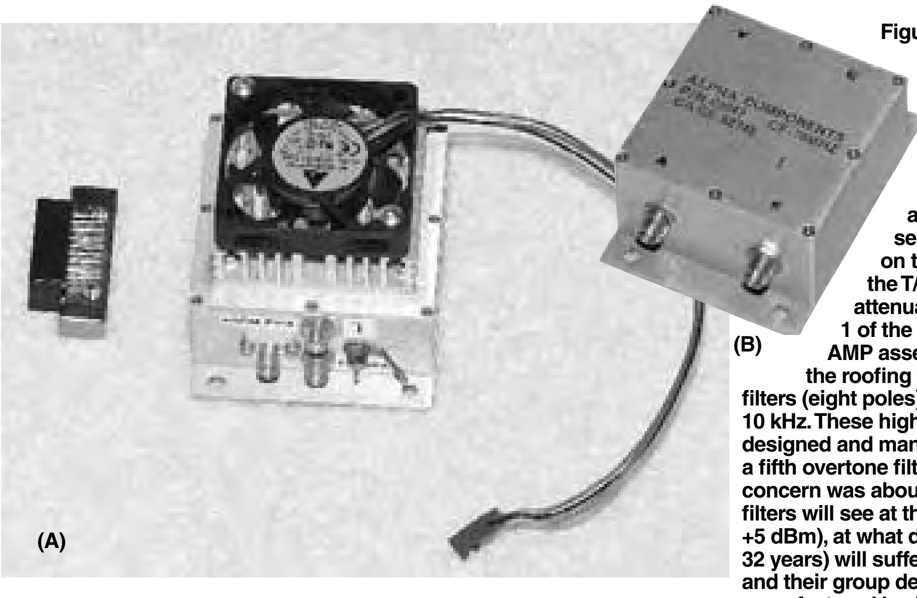


Figure 13 — The physical implementation of the BILAT AMP assembly is shown in Part A. Two back-to-back class A CA2832 amplifiers (one shown at left for size) are packaged together in this assembly. They are passively isolated from each other via a splitter/combiner assembly which provides 20 dB of natural isolation between receive and transmit functions. Switched 24 V dc is selectively provided to the amplifiers depending on the receive or transmit function selected by the T/R assembly via the IF75BC T/R relay. BIPA attenuation is inserted as shown in Figure 2 of Part 1 of the article. The schematic diagram of the BILAT AMP assembly is shown in Figure 14. Part B shows the roofing filter FL75 assembly. It contains two four-pole filters (eight poles) with a 3 dB bandwidth of approximately 10 kHz. These high intercept filters have been especially designed and manufactured for the *Star-10* by Temex Inc. Initially, a fifth overtone filter set was designed and tested. The initial concern was about the maximum amount of RF drive level these filters will see at this point in the system (approximately +5 dBm), at what duty cycle, and how their aging (calculated at 32 years) will suffer under these conditions, their insertion loss and their group delay properties. A second set was designed and manufactured by Alpha Components Inc., using a fundamental Gaussian design, which can provide better resistance to high drive levels.

from part 1 of the article). Thus, the first roofing filter is different in design than the second roofing filter.

The roofing filters assembly contains two four-pole filters (eight poles composite) with a 3 dB bandwidth of approximately 10 kHz. These high intercept filters have been especially designed and manufactured for the *Star-10* by Temex Inc. Initially, a fifth over tone filter set was designed and tested. The initial concern was about the maximum amount of RF drive level these filters will see at this point in the system (approximately +5 dBm maximum), at what duty cycle, and how their aging (calculated at 32 years) will suffer under these conditions, their insertion loss and their group delay properties. A second set was designed and manufactured by Alpha Components Inc., using a fundamental Gaussian design which can provide better resistance to high drive levels. Although a narrower bandwidth was desirable, at 75 MHz, a 10 kHz bandwidth was the best that could be done considering all other design criteria.

It should be noted that despite popular belief, narrowing bandwidth in roofing filters for up-convert transceivers, although very desirable, it is not by far as important as creating crunch proof front ends such as done in IF75BC. Roofing filters of 3 to 4 kHz bandwidth at 75 MHz that withstand high RF levels are hard to realize and manufacture consistently. High dynamic range 75 MHz roofing filters with a 3 dB bandwidth of 10 kHz and high intercept points are, however, possible. Reducing the first IF frequency to a lower frequency, can ease the design of these filters at the cost of more demanding front end filtering to cope with image and spurious rejection. Going to low first IFs of, say, 9 MHz

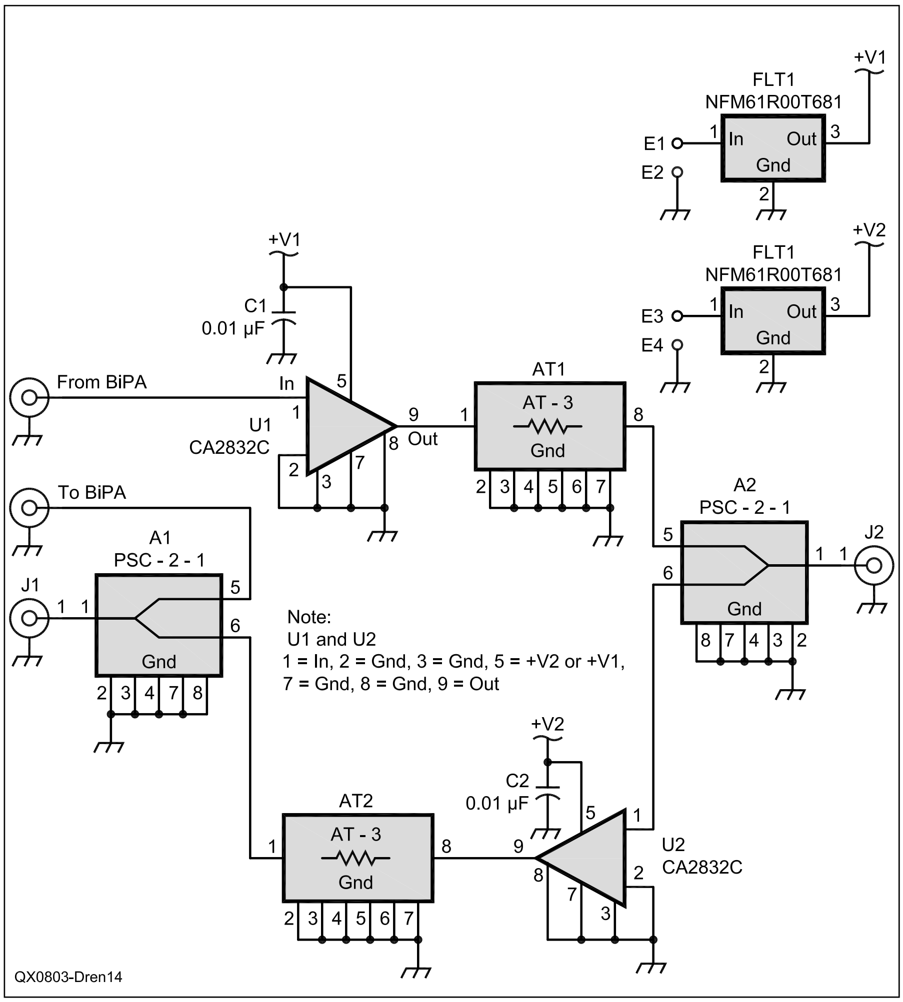


Figure 14 — This is the schematic diagram for the BILAT AMP assembly. This circuit provides high dynamic range selective amplification - bilateral functionality with automatic passive isolation (without using relays) between the active section and the off section, depending on whether the receive or transmit function is selected. The customary 3 dB impedance matching pads at the output of the amplifiers were later eliminated in the interest of gain and noise figure.

can allow for narrow roofing filters of 2 to 3 kHz (compatible with the ultimate bandwidth required of SSB signals); however, the entire idea of a high performance general continuous coverage transceiver can be thrown out the window, resulting in a compromise — channelized band-only, coverage.

Returning to the BILAT AMP assembly, the AT1 and AT2 pads seen in the BILAT AMP have been provided for amplifier matching. However, after long experimentation, they have been removed from the circuit in the interest of gain and noise figure improvements.

The output of the second section of FL75 is input to the IF9BC assembly along with the wide (500 kHz) 75 MHz IF signal intended for spectrum analysis (see Figure 2 in Part 1). The IF9BC assembly is the second bilateral converter which provides 9 MHz receiver IF signals to IF9RX and accepts 9 MHz transmitter IF signals from IF9TX. The wide band 9 MHz IF is further input to IF9NB, which in turn, provides oscilloscope, spectrum analyzer and noise blanker functions for the transceiver. Again, this is shown in the block diagram in Figure 2 of Part 1.

Looking at Figure 15, the two 75 MHz paths are input at J1 (wide) and J3 (narrow) to be converted to 9 MHz IFs separately via two independent high level mixers paths (Mix 1 and 2) in IF9BC using class II, TAK-3H mixers as shown.

Figure 15 shows the 84 MHz fixed frequency LO coming from the MRU (master reference unit) / PLXO, which is filtered and amplified by a class A amplifier and enters the IF9BC at J2. The signal is split by the A1 splitter (another PSC2-1) and is presented equally to the two TAK-3H mixers with a level of +17 dBm. The top mixer IF output is filtered through a wide bandwidth band-pass filter, and is finally amplified by AR1 (a MAR-8 device) to be output to the IF9NB assembly at J4. The narrow-band 9 MHz IF (with a bandwidth equal to the composite bandwidth of the two 75 MHz roofing filters at FL75) coming from MIX2 (the other TAK-3H mixer) is conditioned via the diplexer circuit of L10, C16, R5, L9 and C15, and is split by A2. The first half is output via a 1.5 dB pad through J5 to go to the narrow band receiver IF, IF9RX. The other half goes through another 1.5 dB pad and J6 to be connected with the narrow band transmitter IF when activated. I will explain more about this in Part 3.

I will now discuss the previously mentioned BIPA function using a Pi configuration PIN attenuator provided on IF9BC. This attenuator provides adjustable front panel and first IF/RF gain and noise blanking gating, coming from the IF9NB. It could also be used as a second AGC loop (not implemented yet).

In Figure 15, the 75 MHz input coming from the BILAT AMP is at J7. The attenuated output resulting from the BIPA circuit is available at J8. Control is provided via E2A and B. The BIPA attenuator function is packaged on a 24 pin PC board layout which follows a 24 pin IC module physical design approach. A picture of the BIPA assembly is shown in Figure 16. The schematic diagram of the assembly is shown in Figure 17.

Looking at Figure 17, BIPA uses four voltage controlled 5082-3080 PIN diodes in a Pi configuration. The design was inspired by Raymond Waugh's article in *Microwave Journal* (reference 13). This design approach provides very good impedance matching and flat attenuation over a wide frequency band and can be used in many applications. In fact, I used this circuit in the 9 MHz transmit IF as a CW drive controller as we will discuss later in Part 3.

This attenuator design is very good. After extensive testing at 75 MHz, it was found that with a 3.5 V bias at pin 24 and a control voltage of 0.3 V dc to 10.2 V dc at pins 10, 11, and 12, a range of 43 dB (-45 dB to –2 dB minimum insertion loss) of attenuation can be obtained. Less than 2 dB insertion losses can be obtained with higher control voltages according to reference 13. With the circuit operated at 0 dBm (a rather high level) the third order IMD was -65 dB; at +10 dBm, third order IMD was -50 dB. Additional tests were conducted using 20 kHz tones spacing at 9 MHz (for the IF9TX function) with better results (-70 dB). The BIPA control on *Star-10*, with improved attenuation characteristics can be used not only for manual gain control, but also for muting the IF chain as commanded by the noise blanker. It can also serve as the second AGC control loop in the middle of the receiver chain, for an improved AGC system.

It was found that the minimum insertion loss of the BIPA circuit as applied in the *Star-10* system is about 2 to 3 dB (depending on cables and connectors used). When plugging this into the dynamic range analysis from Part 1, it can be seen that the MDS can be improved if this minimum insertion loss number could be reduced further. If implementing this circuit, a special effort should be made to further reduce its minimum insertion loss through increasing the bias voltage to the rail. This proved helpful in improving the MDS performance. An MDS of –136 dBm (versus the initial –132 dBm) was obtained by improving the minimum insertion loss and/or shorting out the BIPA circuit. This circuit can use a shorting feature utilizing a miniature RF relay similar to the one implemented in the preamp from the IF75BC assembly. The BIPA circuit is a remarkable circuit with outstanding attenuation range and IMD performance.

Master Reference Unit (MRU) / PLL Oscillator (PLXO84)

Next, I will direct our discussion from the receiver and transmitter signal path to the coherent local oscillators (LO) system used in the transceiver. As I previously explained in Part 1, *Star-10* is a "fully coherent" or "fully synthesized" system. This means that all local oscillator frequency sources in the double conversion superheterodyne implementation are locked to a single high stability - high spectral purity source whose performance is reflected in the total long term stability and phase noise performance of the system and is directly translated into the receiver's and transmitter's performance. A high performance master oscillator is required to provide reference frequencies for the synthesizer and all LOs. This master frequency source is the MRU (master reference unit) which generates the 84 MHz reference frequency local oscillator to be used further by the synthesizer (FRU) – FSYNTH and also as a direct fixed LO for converting the 75 MHz bilateral IF to the 9 MHz bilateral IF in IF9BC. Thus, the 84 MHz - MRU LO serves as both, a high quality reference for the two DDSs in the FRU - FSYNTH, as well as a high quality fixed LO for the second conversion. A fully coherent system with equally good phase noise performance at all mixer ports results.

Before going into the circuit description of the MRU, it should be noted that in calculating the phase noise contributions of all LOs in a complex coherent RF system such as *Star-10*, a careful synthesizer analysis should be performed to insure that they are all fully compatible with each other and with the MDS - phase noise and spurious performance of the radio itself. This means that synthesizer performance at all receiver/transmitter LO ports should be equally good throughout as phase noise translates directly dB per dB (minus the mixer loss) into the MDS of the radio within the IF band-pass of interest. Many receiver and transceiver designers do not take this fact into consideration as witnessed by receiver MDS being sometimes obscured (phase noise limited) by the converted poor phase noise. This rule also applies to frequency doublers of lower reference frequencies (for example 32 MHz × 2 for 64 MHz) being commonly used to obtain master reference frequencies, implementation that loses phase noise performance by 6 dB (20 log 2) through the doubling process by the time it gets to the synthesizer and reflects badly in the LO outputs.

Synthesizer design should start with the highest technologically feasible reference frequency and dividing it down from there if necessary (not multiplying up as some companies do) and partitioning the synthesis for

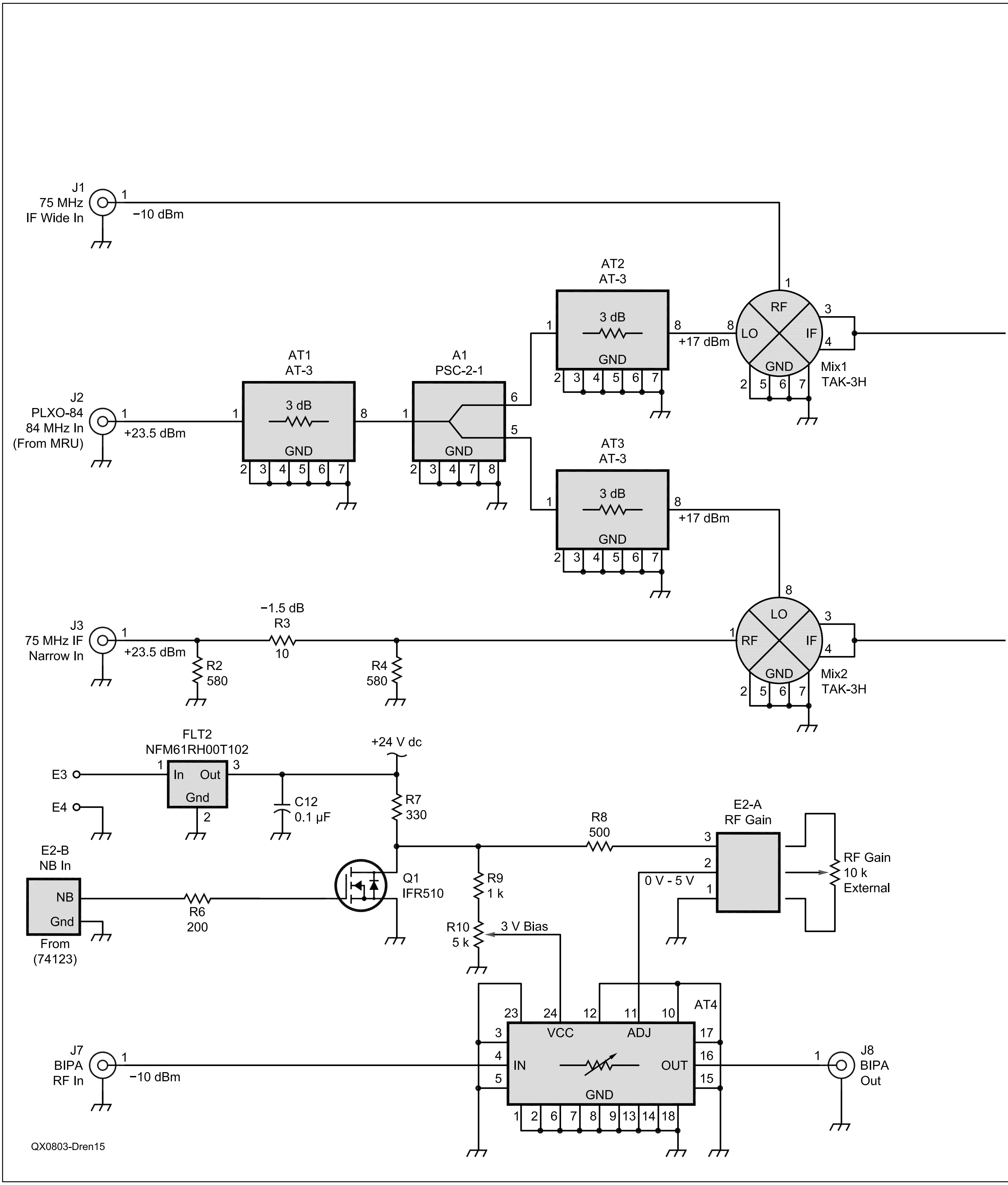
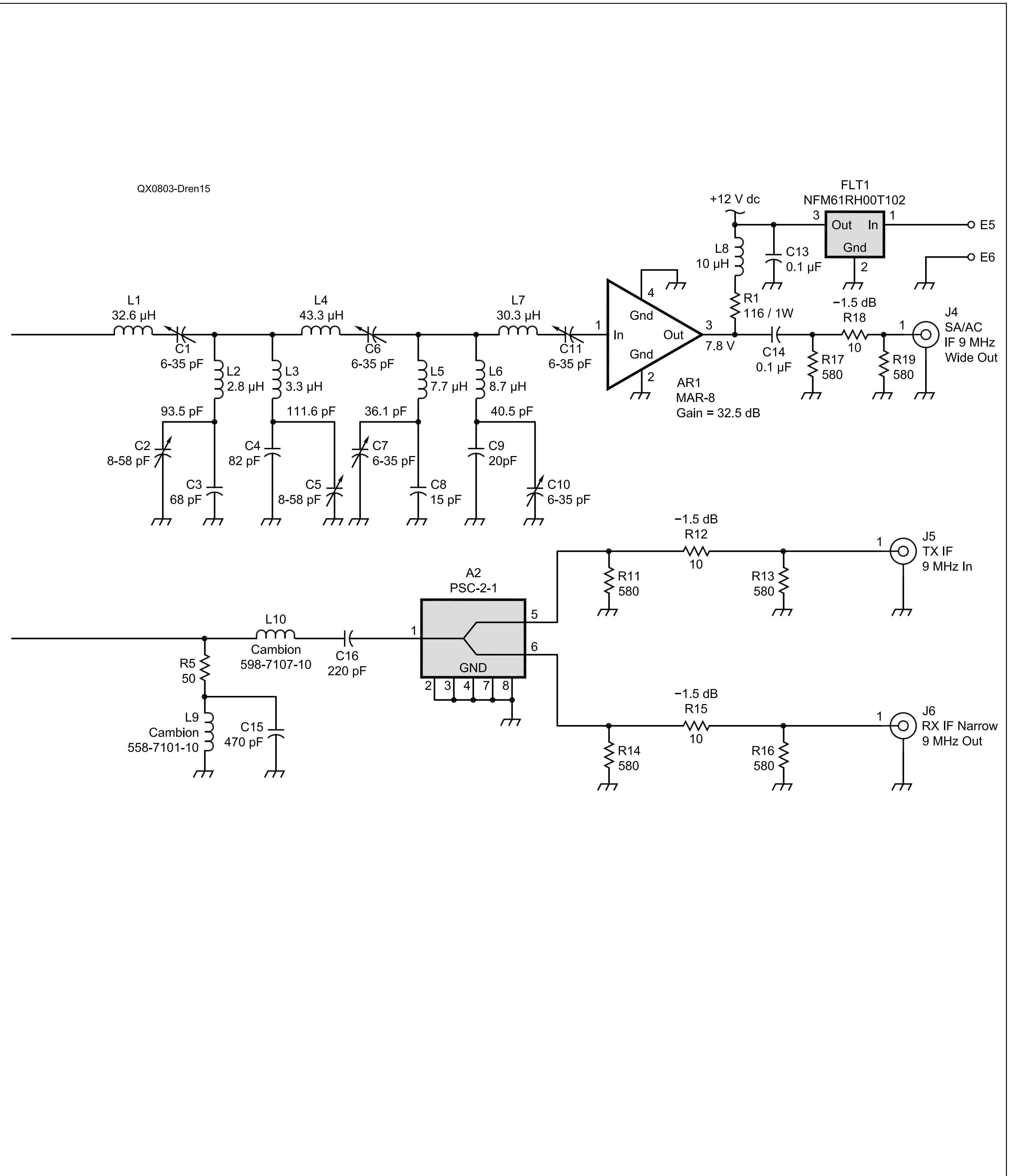


Figure 15 — This schematic diagram shows the circuit for IF9BC, the 9 MHz IF/bilateral converter.



QX0803-Dren15
+12 V dc
FLT1
NFM61RH00T102
3
Out
In
1
Gnd
2
E5
E6
L8
10 µH
C13
0.1 µF
L1
32.6 µH
L4
43.3 µH
L7
30.3 µH
C1
6-35 pF
C6
6-35 pF
C11
6-35 pF
4
Gnd
1
In
Out
3
Gnd
2
R1
116 / 1W
7.8 V
C14
0.1 µF
−1.5 dB
R18
10
R17
580
R19
580
1
J4
SA/AC
IF 9 MHz
Wide Out
AR1
MAR-8
Gain = 32.5 dB
L2
2.8 µH
L3
3.3 µH
L5
7.7 µH
L6
8.7 µH
93.5 pF
111.6 pF
36.1 pF
40.5 pF
C2
8-58 pF
C3
68 pF
C4
82 pF
C5
8-58 pF
C7
6-35 pF
C8
15 pF
C9
20pF
C10
6-35 pF
−1.5 dB
R12
10
R11
580
R13
580
1
J5
TX IF
9 MHz In
A2
PSC-2-1
5
1
6
GND
2 3 4 7 8
L10
Cambion
598-7107-10
C16
220 pF
R5
50
L9
Cambion
558-7101-10
C15
470 pF
−1.5 dB
R15
10
R14
580
R16
580
1
J6
RX IF Narrow
9 MHz Out

the various conversions such as to be fully comparable and balanced between all conversion stages. It does not do a system any good to have a good synthesizer as the first LO, while the second and third LOs in the multiple-conversion RF system are inferior in phase noise performance. The composite results will always reflect the worst LO performance.

The *Star-10* MRU schematic diagram is shown in Figure 18. The actual MRU assembly implementation is shown in Figure 19. Looking at Figure 2 of Part 1, it can be seen that the MRU consists of a 10 MHz OCXO providing the system's long-term stability of 1×10^{-8} after a 30 seconds warm-up, and an 84 MHz PLXO, locked to the stable 10 MHz OCXO for high Q – good phase noise performance of the 84 MHz master reference.

Looking at Figure 18, the *Star-10* MRU utilizes an 84 MHz - precision cut (0.001%) fifth overtone Quartz crystal (X1) with one side of the crystal grounded in a phase-locked series resonant Colpitts oscillator arrangement comprised of Q1 (2N5179), L2, L3, C3, C4, R2, R3 and R4. The Colpitts approach was chosen because of its well-known circuit stability while the 0.001% Quartz crystal cut was chosen to guarantee initial start-up almost on frequency before locking occurs. C3 and C4 are high Q, silver mica capacitors customary of the Colpitts implementation.

Looking at Figure 18, the 84 MHz Colpitts oscillator is initially tuned within its narrow resonance range via L2 and L3, which were calculated to resonate the Colpitts circuit on the fifth overtone of the crystal. Additional tweaking was required to bring the circuit into resonance due to board stray elements with L3 being the key-tuning element. This coil is wound using seven turns of #20 wire on a ¼ inch molded plastic form and using a high-Q aluminium core as an initial frequency control element. L2 is wound in a similar fashion. More detail about this kind of circuit and its PLXO implementation can be found in reference 14, which is available on my Web site listed at the end of this article.

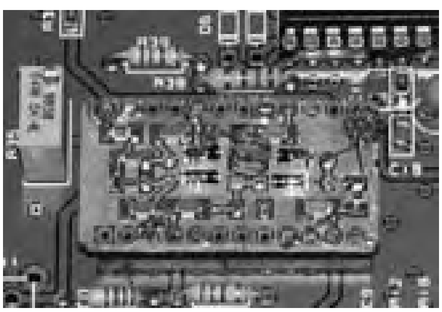


Figure 16 — Actual implementation of the BIPA Pi attenuator used in the IF9BC and the IF9TX assemblies.

The initial free running 84 MHz oscillator is digitally divided down by 84 for a 1 MHz square wave reference signal to be phase compared against a 1 MHz precision frequency signal obtained from the 10 MHz OCXO, as compared against the 10 MHz WWV signal. Upon power on of the *Star-10*, the default-received frequency is the 10 MHz WWV. An exclusive OR phase detector is used to obtain a dc correction signal which is fed back to the 84 MHz Colpitts oscillator via a simple loop filter and a varactor.

Here is how it works. Upon applying power to the MRU assembly, the high performance, low phase noise Colpitts Quartz oscillator starts up almost on frequency due to its 0.001% precision cut. The clean sine wave generated is further amplified by Q2, a 2N5109 transistor. The signal is then filtered using a similar 84 MHz Quartz crystal at X2 and is presented to the divide by two digital divider U1, a UPB1509. This high quality chip has analog to digital conditioning circuits, which allow for a clean 42 MHz signal to be produced. The 42 MHz analog signal is further conditioned/filtered in the IC for extremely low jitter, only to be filtered again via a 42 MHz tubular Quartz crystal filter at X3. The signal is finally presented to U2, a MAX999 low jitter comparator. The threshold of this chip is adjusted via a ten-turn potentiometer, R10. The MAX999 comparator is billed to guarantee a 4.5 ns propagation delay time at 100 MHz. This implies low jitter performance with rise times in the range of 2 ns or less, but experiments comparing the 84 MHz directly through this device showed a relatively noisy signal. Thus, the divide by two conditioning resulted. Using a 42 MHz (less than half its frequency spec) signal into the comparator showed superior and stable (low jitter) results.

The clean 42 MHz square wave signal at U2 pin 1 is further presented to a digital divider string comprised of U3 and U4, two 74161 chips for a divide by 42 (7 and 6) function. A clean 1 MHz square wave results from the 84 MHz Colpitts oscillator, which is further presented to U9A, an exclusive OR phase detector. Further signal conditioning is achieved using U6, a high-speed 54S00 used as sequential gates. The other side of the phase detector is presented with a highly accurate 1 MHz comparison signal derived from the 10 MHz OCXO through another MAX999 comparator and a 50% duty cycle – divide by 10, IC at U8, a 74LS290 part.

It should be noted that the exclusive OR phase detector was chosen on purpose because of its narrow Pi/4 capture range which is exactly what is needed to lock a 0.001% deviation Quartz crystal over the operating temperature range of interest. Using a wider phase detector would result in more searching and additional jitter translating into inferior phase noise performance (something some engineers never learn). Exclusive OR phase detectors need 50% duty cycle digital signals, and locked condition is achieved when the two reference signals are out of phase by 90 degrees. These conditions are fully achieved in the *Star-10* MRU design

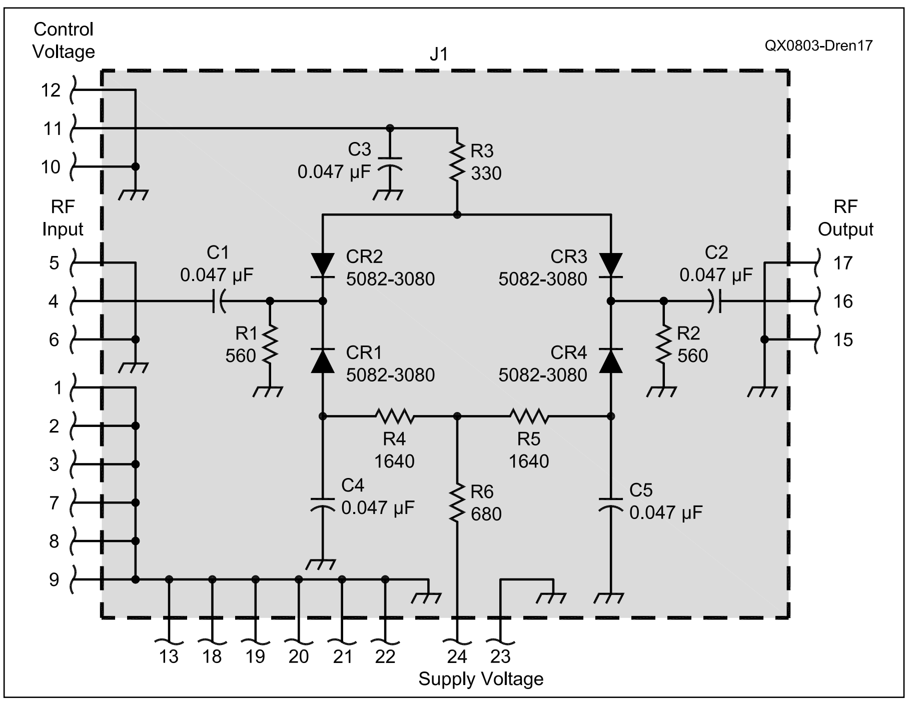


Figure 17 — This is the BIPA circuit diagram.

(note: A quieter mixer type phase detector was briefly considered, but found unnecessary since superior phase noise performance was already achieved with the simple exclusive OR design – see Specification table in Part 1).

The loop correction voltage is obtained at U9A pin 3. The signal is applied through the loop filter comprised of R11, R12 and C19 to the varactor CR1, a BB109. The loop correction signal (2.5 V dc when locked) is fed back to the 84 MHz Colpitts oscillator at the point between C3 and C5 which also serves as the output point of the locked 84 MHz oscillator to be amplified by Q3, Q4, Q6, and filtered by X4, X5, over two channels to provide +10 dBm to +13 dBm fixed reference signals to FSYNTH and serve as a second LO drive in IF9BC. Two additional fifth order tubular narrow band pass filters visible in Figure 19 help reducing further any harmonic spurious content.

It was initially feared that the 1 MHz reference square waves would generate multiple markers at every MHz throughout the HF range. Because of the comprehensive filtering, used, this has not been the case.

For more in depth information on the works of a PLXO MRU and its exclusive OR phase detector, please refer to references 14, 15 and 17.

Operation of the MRU is simple and automatic. Upon turning the power ON to the *Star-10* transceiver, the loop searches within the first 30 seconds for the 10 MHz OCXO signal, which is forced into a quick, warm up mode (the oven heaths up). The 84 MHz signal searches back and forth quickly at a decreasing frequency of approximately 10 Hz and down until the oven in the 10 MHz OCXO reaches its internal temperature (over 100 degrees F) and an exact 1 MHz reference signal is obtained and heard by the receiver beating against the 10 MHz WWV signal. A front panel yellow LED reports to the operator this lock-up process. At this point (MRU locked), the receiver can be redirected to the frequency of interest via the keypad, or via the optoencoder using the proper digit underscore marker on the main dial. All LOs in the *Star-10* are now coherent with the MRU and WWV within 1×10^{-8} and operation can begin. The radio is now guaranteed to be exactly on frequency in receive or transmit regardless of where it is tuned within the 1.8 MHz to 30 MHz range. No drift.

Frequency Reference Unit (FRU) Frequency Synthesizer - (FSYNTH)

The frequency synthesizer in the *Star-10* transceiver is a microwave DDS-Driven PLL running from 770 MHz to 1050 MHz. The idea of DD-Driven PLL is not new. I introduced this idea at RF Expo – 1988, in Anaheim, California (see reference 15). Since then, the majority of transceivers on the market use this concept to generate high-resolution local oscillators frequencies. The synthesizer in *Star-10* goes a step further by generating the LO frequencies at ten times the required frequency range, or 770 MHz to 1050 MHz for improved phase noise performance after a division by 10, which facilitates a 6 dB improvement at the divided down 77 MHz to 105 MHz. This design takes advantage of the reduction in percentage bandwidth offered by the microwave design by using a single VCO (instead of four). The FSYNTH design has been discussed in detail in references 16 and 17. Additional information can be found in reference 18. The schematic for the FSYNTH assembly is shown in Figure 20 and its physical implementation is shown in Figure 21.

Looking at Figure 20, the FSYNTH assembly uses two DDSs, both AD 9850 to generate the variable PLL reference for the DDS-Driven PLL LO as well as the BFO LO. The 50-ohm 84 MHz reference signal coming from the MRU PLXO is input to the FSYNTH assembly at J1. From this point on, it is equally distributed between the two AD 9850 DDSs at pins 9 of U1 and U2. The word-clock commands information for both DDSs coming from the DFCB command and control assembly are input at J1. The command and control assembly will be discussed later. The resolution of the top DDS (U1) is 1 Hz and results in 10 Hz after it gets multiplied by 10 in the PLL loop of the DDS-Driven PLL part of FSYNTH. The highly filtered (to prevent spurious) BFO DDS has a resolution of 10 Hz. The ultimate resolution of FSYNTH as reflected in the transceiver's ultimate resolution from 1.8 MHz to 30 MHz is 10 Hz. For a much more in depth explanation of how the FSYNTH assembly works, please refer to reference 17, page 5. This reference is available on my Web site, which is listed at the end of this article.

Although new and improved DDS devices have evolved since the introduction of the AD9850, the fact remains that spurious performance is still the main challenge in DDS systems used as simplistic direct synthesizers, despite new and clever noise cancelling techniques that have been recently introduced. (See Analog Devices AD9959 Application Note: **www.analog.com/UploadedFiles/Data_Sheets/AD9959.pdf**, p 11.)

As such, the AD9850, if used properly, remains the workhorse of the Analog Devices family of DDS ICs even after all these years. An AD9850 DDS device used in a well-controlled, tight-loop, DDS-driven PLL can indeed exceed the spurious performance of simplistic DDS-only synthesizers using even the most modern DDS devices.

The secret of this superior performance lays in a combination of design parameters, primarily in choosing a correct Nyquist reference frequency (References 15, 16, 17), and the proper interface of the DDS with the PLL phase detector, combined with a well designed loop filter in the PLL.

The FSYNTH performance has been improved since its original design through constant tweaking of the loop filter and a better selection of parts in the microwave divider section and the squaring circuits. This design is capable of -133 dBc/Hz performance from 2 kHz through 20 kHz offset at the divided down output. This performance has been tested and documented as shown in Figure 22. Further phase noise improvements will be discussed in Part 3.

Additional improvements in phase noise performance can be obtained by altering the loop bandwidth and other circuits at the cost of other parameters such as end-to-end synthesizer lock-up split operation and others.

Command and Control Assembly (DFCB)

The command and control assembly - DFCB is the heart of the *Star-10* transceiver. It provides the smarts and the friendly user interface for the system. The system control is achieved through the microprocessor board (part of DFCB) which houses the PIC-17C44 chip discussed in Part 1, its associated hardware, software, and the back-light LCD display assembly viewable through the front panel. This is packaged together on the DFCB, and is used together with the keypad data entry board and the optoencoder and all other user interfaces and controls located behind the front panel of the transceiver as shown in Figure 23.

The command and control system addresses all frequency and mode commands in the FRU — FSYNTH, as well as the various associated frequency selection commands to the half-octave front end filter banks, the ultimate bandwidth and mode selection commands for the receiver IF9RX and IF9TX, the T/R control commands, debouncing delayed Morse code key commands which work in conjunction with the synthesizer split lock-up functions and even display light intensity and multiple sound feed-back tones audible through the receiver's audio amplifier upon depressing keys on the key pad data entry shown on the right side of Figure 23.

The microprocessor code embedded into the command and control system is represented by what the *Star-10* transceiver really does, as commanded from the front panel of the radio. The command and control - DFCB system is primarily capable of addressing

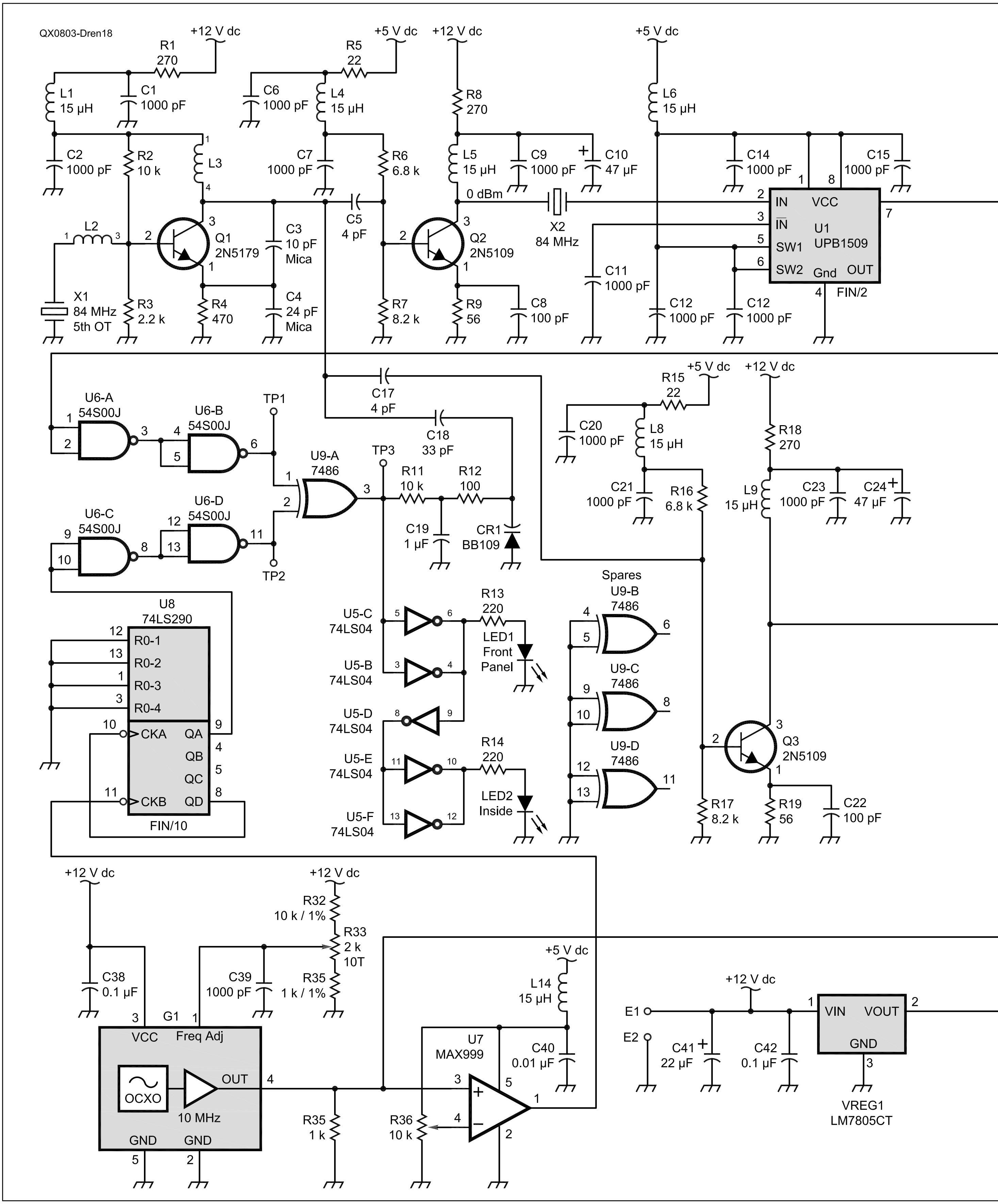
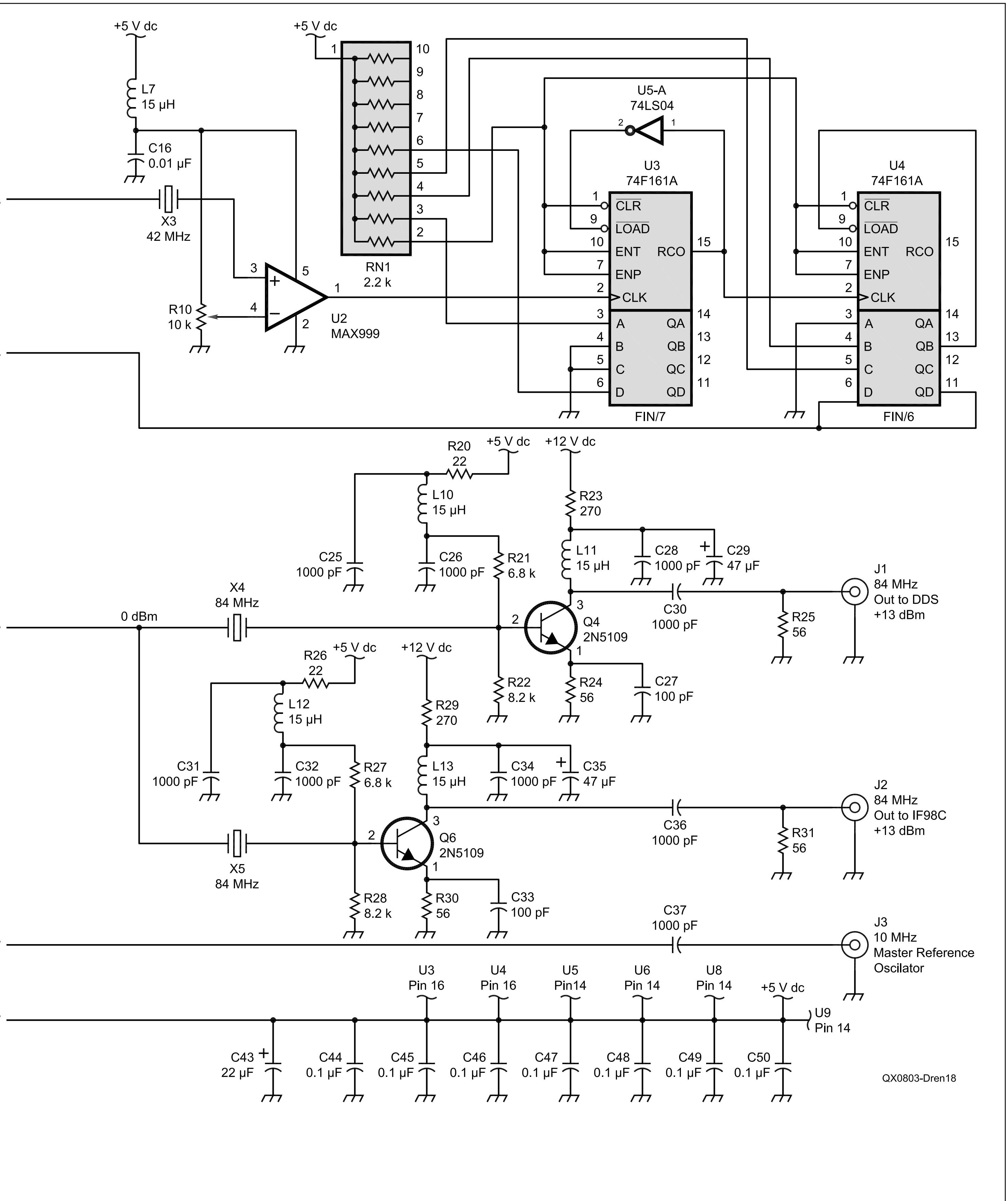


Figure 18 — Circuit diagram of the MRU.



+5 V dc
L7
15 μH
C16
0.01 μF
X3
42 MHz
+5 V dc
RN1
2.2 k
U5-A
74LS04
U3
74F161A
U4
74F161A
CLR
LOAD
ENT
RCO
ENP
CLK
A
B
C
D
QA
QB
QC
QD
FIN/7
FIN/6
R10
10 k
U2
MAX999
R20
22
+5 V dc
+12 V dc
L10
15 μH
R23
270
C25
1000 pF
C26
1000 pF
R21
6.8 k
L11
15 μH
C28
1000 pF
C29
47 μF
J1
84 MHz
Out to DDS
+13 dBm
X4
84 MHz
0 dBm
Q4
2N5109
C30
1000 pF
R25
56
R26
22
+5 V dc
+12 V dc
R22
8.2 k
R24
56
C27
100 pF
L12
15 μH
R29
270
C31
1000 pF
C32
1000 pF
R27
6.8 k
L13
15 μH
C34
1000 pF
C35
47 μF
J2
84 MHz
Out to IF98C
+13 dBm
Q6
2N5109
C36
1000 pF
R31
56
X5
84 MHz
R28
8.2 k
R30
56
C33
100 pF
C37
1000 pF
J3
10 MHz
Master Reference
Oscillator
U3
Pin 16
U4
Pin 16
U5
Pin14
U6
Pin 14
U8
Pin 14
+5 V dc
U9
Pin 14
C43
22 μF
C44
0.1 μF
C45
0.1 μF
C46
0.1 μF
C47
0.1 μF
C48
0.1 μF
C49
0.1 μF
C50
0.1 μF
QX0803-Dren18

either the main loop DDS-Driven PLL or the BFO DDS. The main synthesizer loop (the DDS-Driven phase-locked microwave loop) is controlled through direct keypad entry as taken over by the optoencoder. When in the mode select mode, the keypad controls the microprocessor such that the BFO/DDS-2 follows a fixed programmed function/frequency offsets from the nominal 9 MHz and as changed by the USB, LSB, CW, CWN, AFSK commands requirements. This programmability along with the entire transceiver's frequency sources programmability was previously shown in Table 1 of Part 1. Up/Down arrow commands are used on the keypad to enter RIT and RX and TX - PBT offsets. The PBT function allows selected TX or RX offsets to vary ± 1.5 kHz moving the IF BW and other sources in either side of the zero in either transmit or receive by using the main tuning knob. Once set, the IF PBT remains memorized, to be reset back only by the power off function. The RIT function accessible through the main knob when in RIT mode, allows for ± 9.9 kHz received frequency offset from nominal and gets reset to nominal zero by turning the transceiver power off. The schematic diagram of the DFCB assembly is shown in Figure 24.

Looking at Figure 24, the heart of the command and control system, DFCB is the PIC-17C44 microprocessor at U4. As can be seen, all I/O ports have been thoroughly used by the *Star-10* design. The microprocessor runs at 32 MHz as shown using the Quartz crystal oscillator X1 at pins 19 and 20. The reason for this frequency choice was described in Part 1 of this article series. Harmonics and products of this oscillator are outside of the receiver bandwidth. The switching RF noice produced by the display (which can be heard on a pocket AM Broadcast radio held in front of the display) does not impact the receiver because of the considerable shielding of the assemblies. There is absolutely no impact on the receiver MDS.

The keypad interface is shown on the left side of the drawing. The keys are arranged in a matrix of switches that address the microprocessor through closing user commanded keys via J4 A and B and through the 74HCT138 decoder demultiplexer at U2. Two OPTREX DMC-16230 N - EB displays (DISP 1 and DISP 2) using multiple green LEDs behind a dot matrix LCD for backlighting, are wired and addressed in parallel from the I/O ports as shown. Contrast adjustments are provided through R2 and R3. A switched "bright" function is facilitated by pulling more current through the display LEDs via the IFR510 FET at Q1. The bright command as well as the sound feedback command are implemented via the microprocessor by touch-pushing the main

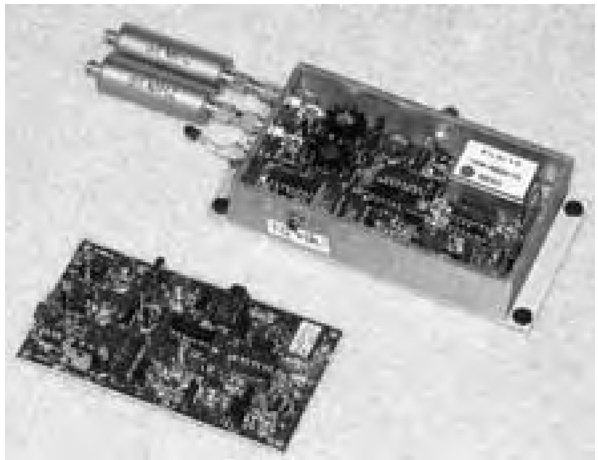


Figure 19 — The *Star-10* MRU assembly uses an 84 MHz PLXO for good phase noise as locked to a 10 MHz OCXO (WWV compared) for long term stability of 1 × 10^{-8}. A simplified version was also developed using a 16.8 MHz TCXO (bottom photo) but was abandoned due to the inferior stability of the TCXO as compared with the OCXO.

tuning knob through the push-push switch provided in the optoencoder. The optoencoder is an inexpensive 32 positions Clarostat unit wired through J2 directly into the I/O ports as shown. The 99 memories function is provided by the permanent memory IC, 25C060 at U1. Memorizing a frequency is easy by using the MR and ENTR functions on the keypad. The memorized frequencies are not erased with power off. They can only be erased by using the keypad and entering a new frequency in an addressed memory number from 1 to 99. The half-octave filters (receiver band-pass and transmitter low-pass) are selected automatically by the microprocessor and output through another 74HCT138 — a three to eight line decoder demultiplexer at U3 and through a tri-state inverting octal buffer, 74HC240 at U6. These logic signals are further carried via connector J5 to the half-octave filter banks via the mother board connectors located on the back of the main shelf as previously discussed. The logic arrangement at U5 A, B, C and D is intended for debouncing functions through the I/O interface connectors. Additional command and control signals are provided from this assembly to the FSYNTH, IF9RX, IF9TX and the T/R assembly via the J1 and J3 connectors. As with all other assemblies in the *Star-10*, proper voltages and regulation are provided via on-board variable and fixed regulators, in this case, a 7805 at VREG1. For reason of simplicity, the three LEDs that work in conjunction with the AIPA selector have not been shown in Figure 24. This completes the DFCB assembly description.

9 MHz Narrow Band Receiver IF (IF9RX)

I will next discuss the receiver narrowband IF — IF9RX. Its design was briefly presented in Part 1 of this series. The ultimate receiver bandwidth requirements are established through the IF9RX assembly and its custom made Quartz crystal filters. Commands are received through the command and control assembly, DFCB. Conversely, the transmitted bandwidth for the SSB/AFSK transmit functions is established through a similar filter bank in the IF9TX assembly. This will be discussed later in Part 3 of this series.

As can be seen from Figure 2 of Part 1, the IF9BC main receiver output is further input to the IF9RX assembly. This IF path achieves the ultimate receiver bandwidth selection and amplification as commanded by the command and control assembly, DFCB.

The IF9RX board provides approximately 100 dB of AGCed gain (80 dB AGC control plus filter insertion loss compensation) using three high dynamic range (+15 dBm IP3) AD-603 logarithmic/linear IF blocks from Analog Devices. This choice was made after an intense search for the right amplifier device. Initially, the old and popular MC-1590 device was considered based on prior art (reference 19). After intense IP3 tests in the KG6NK laboratory using two-tone signals (1.5 kHz apart) at 9 MHz, with and without AGC applied, the IP3 performance of the MC-1590 was found to be inferior. The idea was quickly abandoned.

Several other choices were considered. Among them were the Analog Devices AD600, AD602, AD603, AD604, AD605 and Cougar AGC230. The Cougar device, while offering a third order intercept point of +21 dBm, was too expensive for this application. After ample conversations with Dana Whitlow of Analog Devices, I zeroed in on the AD603, an inexpensive high performance device. This is a low noise device with a bandwidth of 90 MHz, which can be powered from a single 10 V supply. It is a voltage-controlled amplifier, which provides gains of +9 dB to +51 dB (42 dB) and a "linear in dB" accurate and stable range suitable for a linear — in dB — S-meter indicator. It offers a –67 dBm AGC threshold. Its IP3 is +15 dBm. Its noise figure is billed at 8.8 dB. Quick system calculations revealed that if using two AGCed

AD603 devices cascaded with switched in Quartz crystal filters and followed by a third AD603 programmed to compensate for filters insertion loss can provide slightly over 100 dB gain with about 80 dB of AGC. Gain system implications revealed that AGC action and consequently S-meter action would start at approximately – 103dBm signal at the receiver antenna input or an S-3 signal level. This was deemed as a good enough compromise considering the circuit complexity and a linear range of 70 dB shown on the S-meter from an S3 to an S9 plus 40 dB signal level.

Several breadboards were constructed and tested together with Dana Whitlow and Constantin Popescu, (KG6NK) using these ideas, and based on Analog Devices recommendations (see reference 20). An actual to-size first cut board was laid out courtesy of Bruno Santalucia (I6YPK). Because of the 100 dB gain provided by this important board, and the limited board size of 5.5 × 4.5 inches, the IF9RX board had to be laid out again to prevent possible oscillation. A special effort was made by KD7KEQ to provide extra ground stitching for the final layout.

The IF9RX concept was briefly discussed in Part 1 of this series. A block diagram and discussion appears in Figure 5 of Part1. The IF bandwidth selection is provided by four 8-pole crystal filters for a total of 32 possible poles of selectivity. Instead of selecting individual filters as in conventional IF designs, the *Star-10* IF9RX filter assemblies are combined in a cascaded AND function (rather than an OR function) for a total of 32 poles (plus the 8 poles composite roofing filter) of superb selectivity. This cascaded architecture makes the IF9RX a unique design that works in tandem with the system's command and control software.

As shown in Figure 5 of Part 1, two 8 pole crystal filters with a bandwidth of 2.4 kHz are always used at the beginning and the end of the 9 MHz IF chain for good noise management. This idea was inspired by standard RF design procedures and by reference 18. Additional 8 pole crystal filters of narrower bandwidths are inserted or removed between the gain stages (for a maximum of 32 poles in CW Narrow mode) depending on the mode selection and as commanded by the DFCB. The selection is achieved with miniature RF Teledyne relays, just as in the front end of the radio (no diode switching for RF paths in this radio). Automatic insertion loss compensation control is achieved depending on the diverse filters configurations chosen so there is no difference in signal amplitude and S-meter reports when changing filters and bandwidths.

The schematic diagram for the IF9RX is shown in Figure 25 and the actual implementation of the assembly is shown in Figure 26.

Here is how it works. Looking at Figure 25, the 9 MHz receiver IF signal coming from one side of the bottom splitter in IF9BC is input to the IF9RX assembly at J3. It is then passed through the first 8-pole, 2.4-kHz-wide quartz filter, XF1. This filter and XF4 (an exact similar filter intended to limit the noise content of amplifiers) are always in the circuit. Two cascaded AD603 amplifiers U1 and U2 follow the first filter. They are AGCed at point A via the circuit containing Q8, Q9, Q10 and U7A. The AGC signal is derived at U3 as shown. AGC ON/OFF and time constant (FAST/SLOW) functionality from the front panel are provided through J1 along with IF gain and MUTE functions (through Q7). The attack time is fast in all modes (<2 ms) while the fast decay time is 0.5 seconds and the slow decay time is 4 seconds. The output of the AGCed amplifiers at U2 is further cascaded via additional Quartz filters XF2 and XF3. The operator controls the filter selection and insertion loss compensation from DFCB via the keypad depending on the mode and bandwidth selected. The filters are merrily inserted in the circuit or shorted out using miniature Teledyne RF relays as shown. Control signals are applied to U4, U8 and the relays (K1, K2, K3, K4, K5) via J1 and J2 as shown. The output of XF3 is further presented the third AD603 at U3 which inserts fixed gain compensation as set by R33 and R40 depending on the narrow filters selected (XF2 or XF3).

It should be noted that "narrow" means different things in different modes. In SSB for instance, "narrow" means that XF2 (1.8 kHz) was selected, while in CW or AFSK, "narrow" selects XF2 (1.8 kHz) and XF3 (500 Hz) for a total of 32 poles of cascaded selectivity. Conversely, "wide" means different things in different modes: In SSB for instance, "wide" uses XF1 and XF4 (both 2.4 kHz, 16 pole filters) while in CW, "wide" selects XF2 (1.8 kHz) together with XF1 and XF4 for 24 poles of filtering. The intelligence for these selections is actually built into the DFCB assembly and is part of the software design. The computer in DFCB actually understands which mode was selected from the keypad and makes the right decisions accordingly.

Metering functionality by switching from the S-meter function in receive to the RF power meter function in transmit is provided through J2 via K5. IF gain control is wired to the front panel control potentiometer via the J1 connector.

Some of the circuits in IF9RX are powered directly from 12 V dc. The AD603 amplifiers are powered from the +12 V dc input E1 through U5, a programmable LM317 regulator set at 10 V dc. Additional 5 V dc power is supplied to the 75451 line drivers (U4 and U5) via a 5 V dc regulator, U6.

Despite its relatively simple apparent design, the IF9RX assembly has been a challenging IF to implement, because of the very high gain requirements and the relatively small space available on the board. Its novel cascaded functionality has proven to be well worth the extra effort of diverting from the classic "one filter at the time" mode selection of the past.

This concludes Part 2 of this article series. In Part 3, I will discuss the receiver product detector Assembly (PDAF), the transmit / receive (T/R) controller, the 9 MHz transmitter IF (IF9TX), additional assemblies, power linear amplifier, the EMI-quiet switching power supply, putting it all together, the final performance tests and conclusions as well as the lessons learned.

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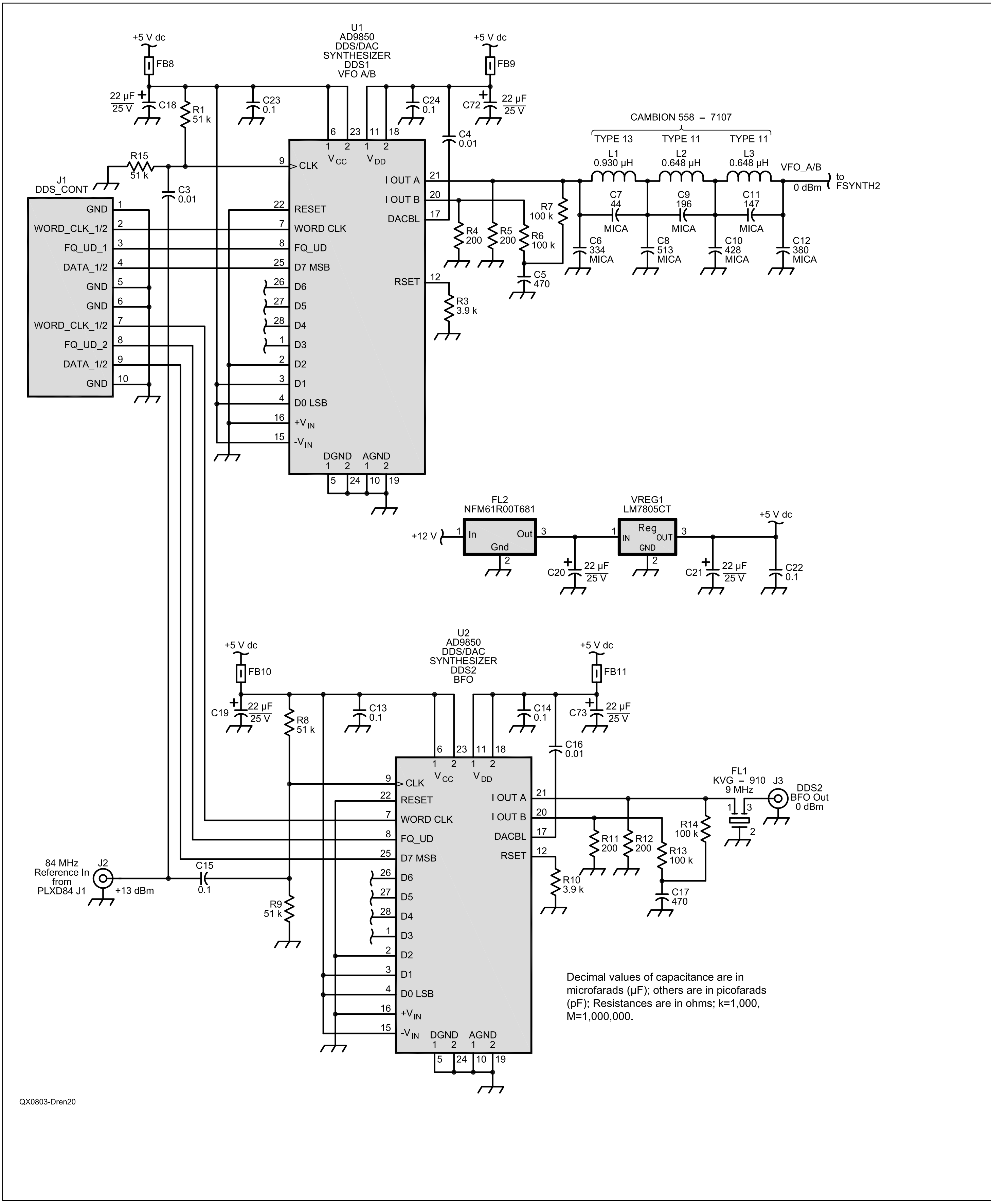
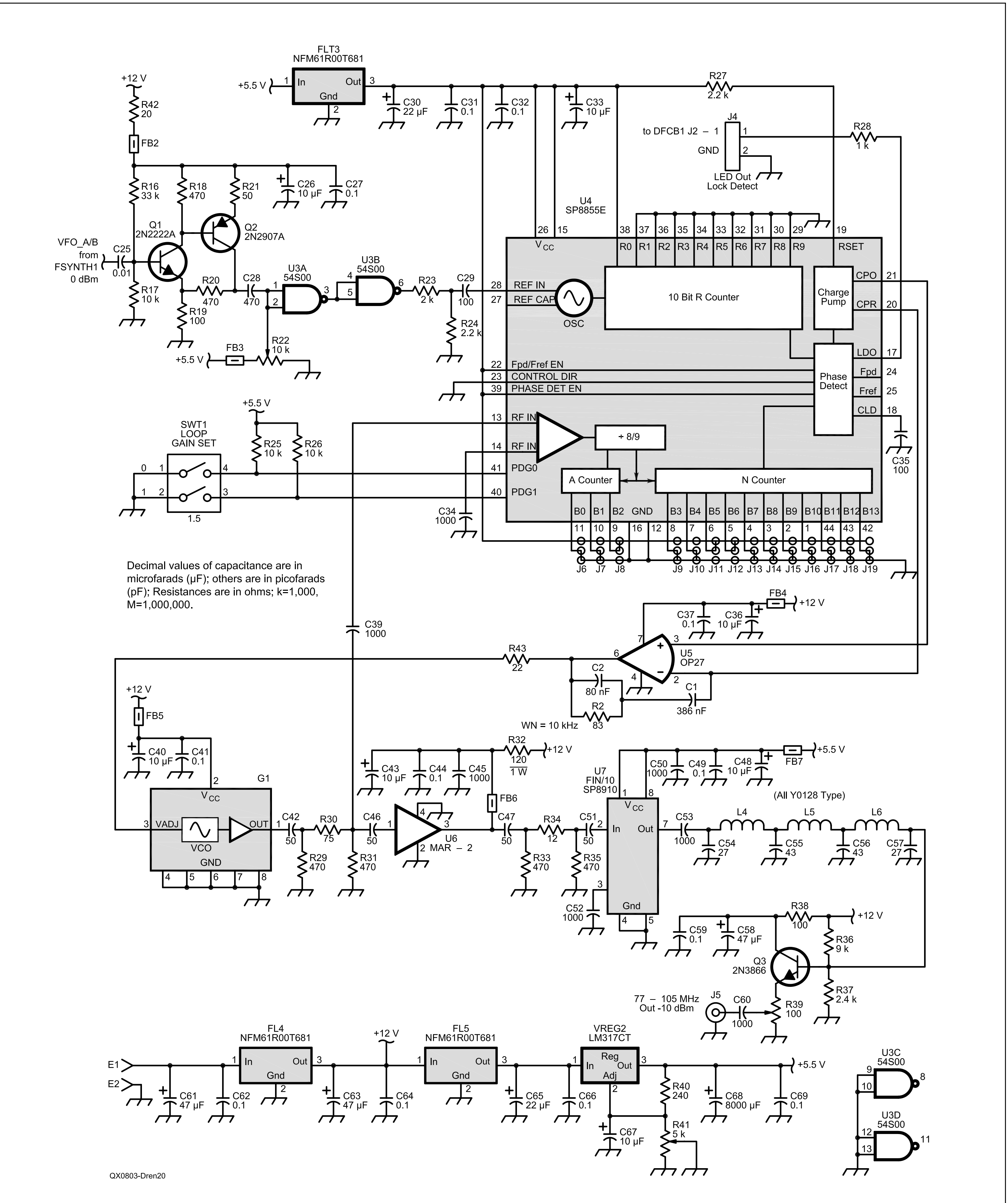


Figure 20 — Schematic diagram for the *Star-10* frequency reference unit (FRU), FSYNTH.


FLT3
NFM61R00T681
+5.5 V
In
Out
Gnd
+12 V
R42
20
FB2
R16
33 k
R18
470
R21
50
C26
10 µF
C27
0.1
C30
22 µF
C31
0.1
C32
0.1
C33
10 µF
R27
2.2 k
J4
to DFCB1 J2 – 1
GND
LED Out
Lock Detect
R28
1 k
U4
SP8855E
Q1
2N2222A
Q2
2N2907A
VFO_A/B
from
FSYNTH1
0 dBm
C25
0.01
R17
10 k
R20
470
C28
470
R19
100
U3A
54S00
U3B
54S00
R23
2 k
C29
100
R24
2.2 k
FB3
R22
10 k
V CC
R0 R1 R2 R3 R4 R5 R6 R7 R8 R9
RSET
REF IN
REF CAP
OSC
10 Bit R Counter
Charge
Pump
CPO
CPR
LDO
Fpd
Fref
CLD
Phase
Detect
Fpd/Fref EN
CONTROL DIR
PHASE DET EN
RF IN
÷ 8/9
PDG0
PDG1
A Counter
N Counter
B0 B1 B2 GND B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13
J6 J7 J8 J9 J10 J11 J12 J13 J14 J15 J16 J17 J18 J19
C35
100
SWT1
LOOP
GAIN SET
R25
10 k
R26
10 k
1.5
C34
1000
Decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); Resistances are in ohms; k=1,000, M=1,000,000.
C39
1000
FB4
C37
0.1
C36
10 µF
R43
22
U5
OP27
C2
80 nF
R2
83
C1
386 nF
WN = 10 kHz
FB5
C40
10 µF
C41
0.1
G1
VADJ
VCO
OUT
GND
C42
50
R30
75
R29
470
R31
470
C46
50
R32
120
1 W
C43
10 µF
C44
0.1
C45
1000
FB6
U6
MAR – 2
C47
50
R34
12
C51
50
R33
470
R35
470
U7
FIN/10
SP8910
C50
1000
C49
0.1
C48
10 µF
FB7
(All Y0128 Type)
C53
1000
L4
L5
L6
C54
27
C55
43
C56
43
C57
27
C52
1000
R38
100
C59
0.1
C58
47 µF
R36
9 k
Q3
2N3866
R37
2.4 k
77 – 105 MHz
Out -10 dBm
J5
C60
1000
R39
100
FL4
NFM61R00T681
FL5
NFM61R00T681
VREG2
LM317CT
Reg
Adj
E1
E2
C61
47 µF
C62
0.1
C63
47 µF
C64
0.1
C65
22 µF
C66
0.1
R40
240
C68
8000 µF
C69
0.1
C67
10 µF
R41
5 k
U3C
54S00
U3D
54S00
QX0803-Dren20

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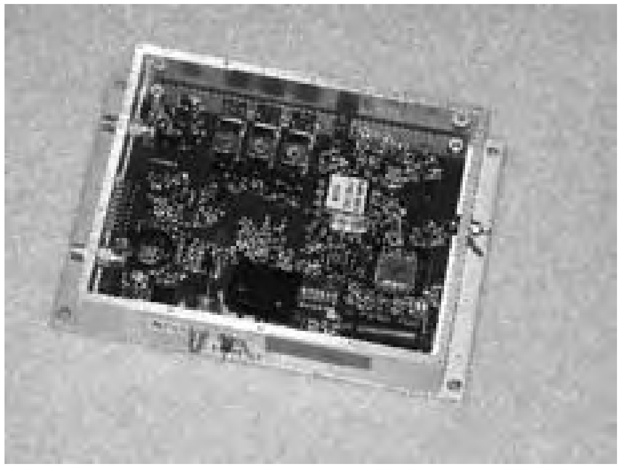

Figure 21 — Actual FSYNTH assembly implementation.

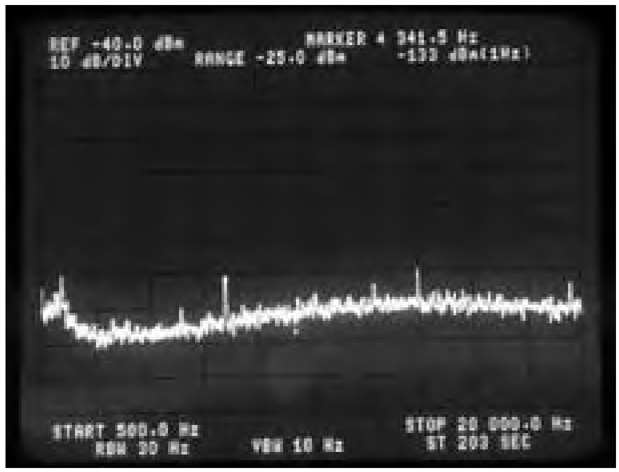

Figure 22 — Phase noise performance of the *Star-10* FSYNTH assembly shows a close in performance of –133 dBc/Hz at 4 kHz. The photo shows total performance from 500 Hz to 20 kHz from the carrier. This test was performed directly at the output of the synthesizer at 89.2 MHz (14.2 MHz). A rather tight loop bandwidth was chosen (see reference 17) and shows the normal "hump" created by the super imposing of the VCO phase noise with the loop bandwidth. The FSYNTH loop bandwidth is optimized here for close in performance (from 500 Hz through 4 kHz) since this noise content is reflected dB per dB through the transceiver's mixers especially in the receiver performance.

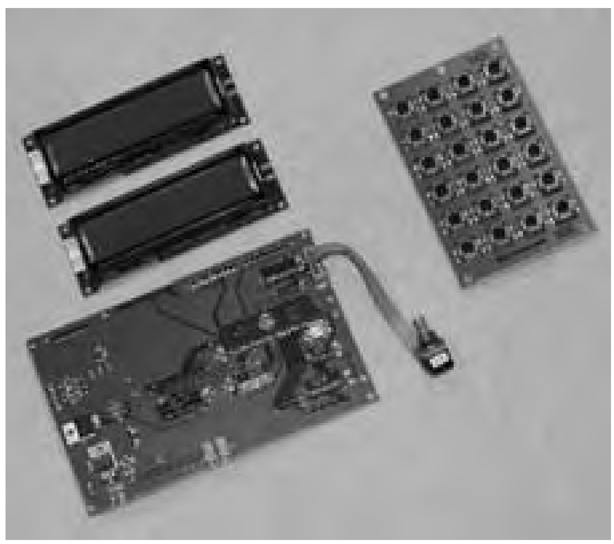

Figure 23 — The command and control assemblies behind the front panel contain the main DFCB board (with microprocessor shown), the optoencoder, the 64 characters displays that plug into DFCB board and the key pad board, all interconnected with ribbon cables. See text.

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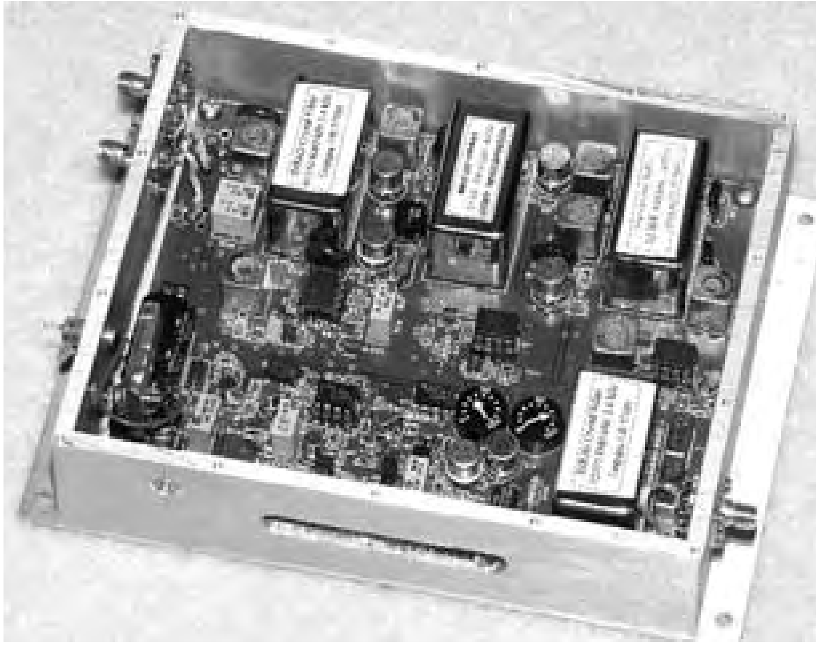

Figure 26 — Actual implementation of the IF9RX assembly. A specific double side ground plane stitched - plated through layout is used to maximize isolation between input circuits and output circuits in order to prevent oscillation in this very high gain (100 dB) assembly. All Quartz filters on the assembly have been expressly manufactured for the *Star-10* by International Filter Company.

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Cornell Drentea, KW7CD, has been a ham since 1957. He has built many radios and transceivers and made his passion for designing "radios" his lifelong profession. As an amateur radio operator, he is known for his extensive RF technology articles in magazines such as ham radio*,* Communications Quarterly, RF Design*, and* QEX*. Professionally, Cornell is an accomplished RF technologist, an engineer and a scientist with over 40 years of hands-on experience in the aerospace, telecommunications and electronics industry. He received his formal education abroad with continuing studies and experience achieved in the United States. Cornell has presented extensively on RF design topics at technical forums such as IEEE, RF-Expo, Sensors-Expo and has given comprehensive professional postgraduate courses in RF receiver design, synthesizer design, sensors and communications. He has published over 80 professional technical papers and articles. He is the author of the book,* Radio Communications Receivers*, McGraw Hill, ISBN 0-8306-2393-0 and ISBN 0-8306-1393-5, 1982. You can find out more about Cornell, on his web site:* **members.aol.com/cdrentea/myhomepage/**

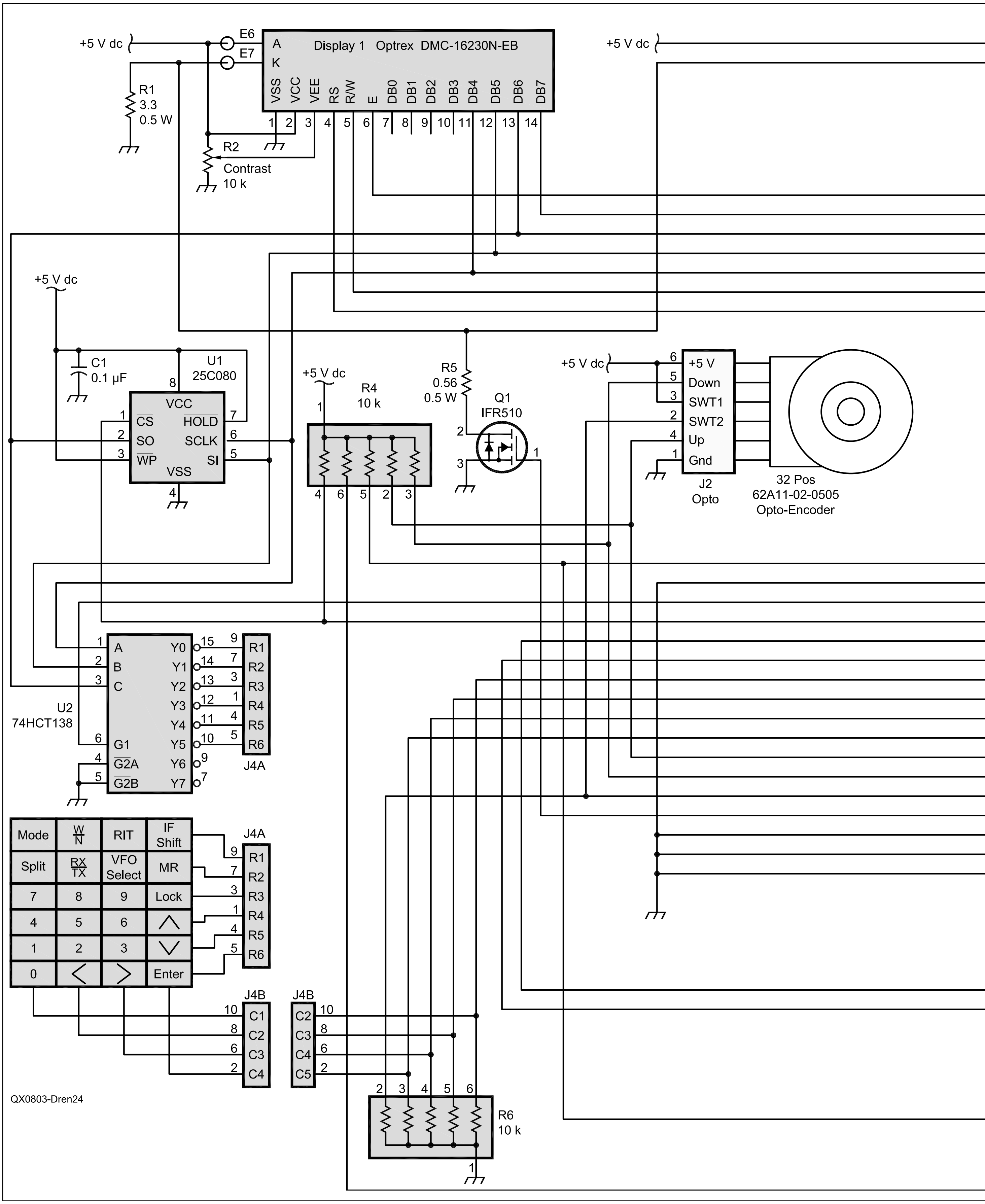
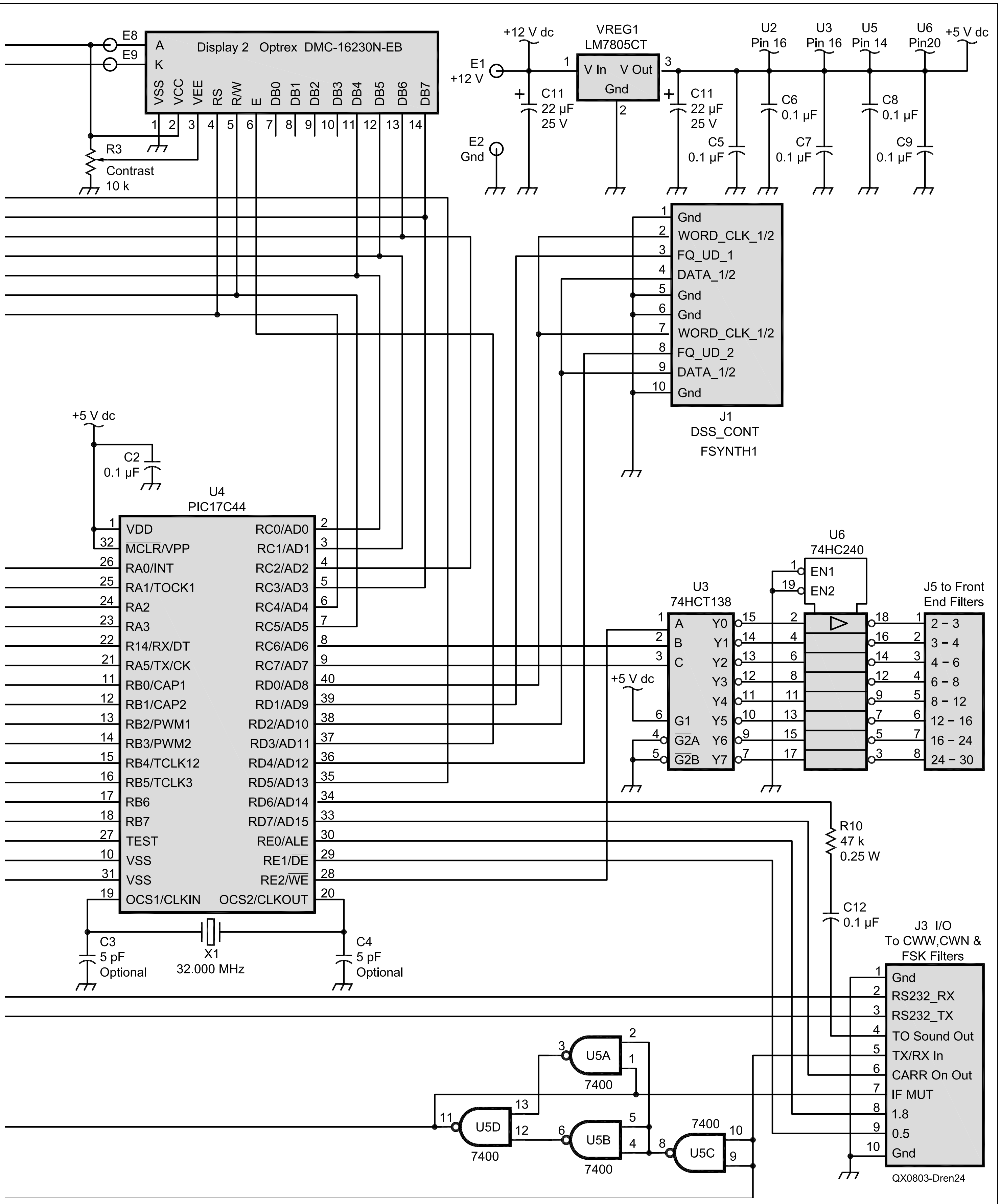


Figure 24 — Schematic diagram of the DFCB command and control system.



Display 2 Optrex DMC-16230N-EB
E8
E9
A
K
VSS VCC VEE RS R/W E DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
R3
Contrast
10 k
+12 V dc
VREG1
LM7805CT
V In
V Out
Gnd
E1
+12 V
E2
Gnd
C11
22 µF
25 V
U2 Pin 16
U3 Pin 16
U5 Pin 14
U6 Pin20
+5 V dc
C5 0.1 µF
C6 0.1 µF
C7 0.1 µF
C8 0.1 µF
C9 0.1 µF
Gnd
WORD_CLK_1/2
FQ_UD_1
DATA_1/2
Gnd
Gnd
WORD_CLK_1/2
FQ_UD_2
DATA_1/2
Gnd
J1
DSS_CONT
FSYNTH1
+5 V dc
C2
0.1 µF
U4
PIC17C44
VDD
MCLR/VPP
RA0/INT
RA1/TOCK1
RA2
RA3
R14/RX/DT
RA5/TX/CK
RB0/CAP1
RB1/CAP2
RB2/PWM1
RB3/PWM2
RB4/TCLK12
RB5/TCLK3
RB6
RB7
TEST
VSS
VSS
OCS1/CLKIN
RC0/AD0
RC1/AD1
RC2/AD2
RC3/AD3
RC4/AD4
RC5/AD5
RC6/AD6
RC7/AD7
RD0/AD8
RD1/AD9
RD2/AD10
RD3/AD11
RD4/AD12
RD5/AD13
RD6/AD14
RD7/AD15
RE0/ALE
RE1/DE
RE2/WE
OCS2/CLKOUT
C3
5 pF
Optional
X1
32.000 MHz
C4
5 pF
Optional
U6
74HC240
EN1
EN2
U3
74HCT138
A B C
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
G1
G2A
G2B
+5 V dc
J5 to Front
End Filters
2 – 3
3 – 4
4 – 6
6 – 8
8 – 12
12 – 16
16 – 24
24 – 30
R10
47 k
0.25 W
C12
0.1 µF
J3 I/O
To CWW,CWN &
FSK Filters
Gnd
RS232_RX
RS232_TX
TO Sound Out
TX/RX In
CARR On Out
IF MUT
1.8
0.5
Gnd
U5A
U5B
U5C
U5D
7400
QX0803-Dren24

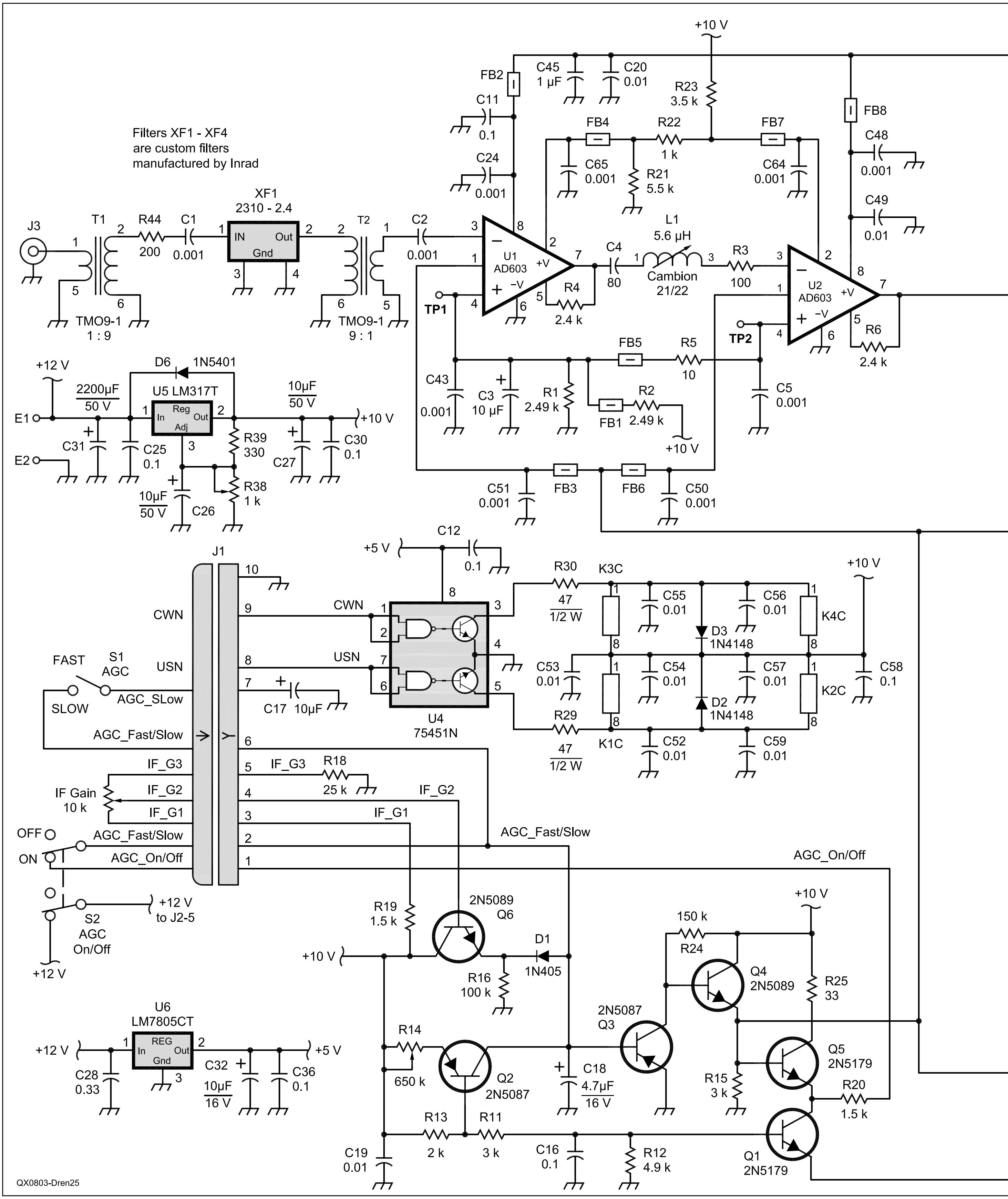
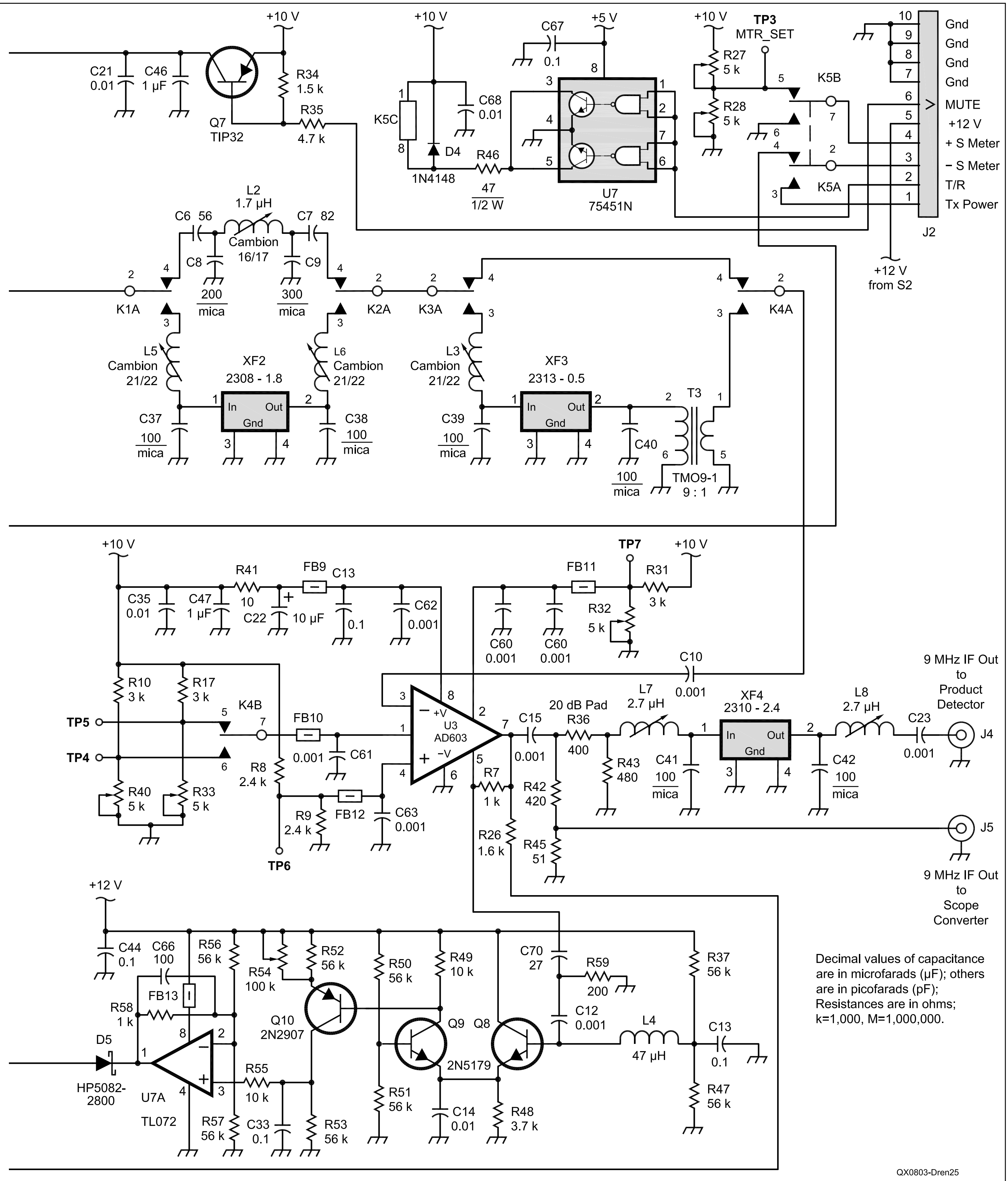


Figure 25 — Schematic diagram of the IF9RX assembly. Two 2.4 kHz - wide filters (one at the IF input and one at the IF output) are always in the circuit. Additional filters for SSB narrow (1.8 kHz) and CW/AFSK narrow (500 Hz) are inserted or shorted out from the command and control DFCB assembly using the keypad and the intelligence built into DFCB microprocessor. Two AD603s are used for AGCed gain and



a third AD603 is used after the 1.8 kHz filter and the 500 Hz filter to compensate for the insertion loss of the selected filters. All filters are cascaded in an AND function rather than selected individually in an OR function, to optimize shape factor and depending on the mode and bandwidth selection. 32 poles of maximum filtering are possible.

Cornell Drentea, KW7CD

cdrentea@aol.com

The *Star-10* Transceiver — Part 3

In Part 3 of this series we conclude with the remaining circuits used in this high-performance transceiver, along with the final test results, which support the specifications presented in Part 1.

KW7CD Photo

This photo shows a back view of the *Star-10* transceiver prototype during final assembly. The sensory electronics are shown on the left, the power linear amplifier assembly (with fans on the heat sink) is in the center, and the master reference unit (MRU) is on the right.

Mission

The *Star-10* transceiver has been a unique research experience into understanding what can be done from the laws-of-physics point of view in receiver and transceiver dynamic range performance. This research has been performed over a period of five years, with parts, technologies and packaging means available to me at the time. The transceiver has been implemented with some unique parts that may no longer be available. The *Star-10* development has been a purely scientific endeavor intended primarily to understand what could be done to achieve ultimate receiver performance. Although the results have been outstanding, slightly better results may be possible using newer technologies and parts. The *Star-10* project was not intended as a product. Its duplication is probably not economically feasible.

Errata

We regret that several errors have crept into the first two parts of this series. In Part 1, the power supply specification incorrectly listed the TX max dc power as 800 VA. The correct specification is 450 VA. Also in Part 1, the caption with the lead photo of the *Star-10* transceiver indicated that the electrical and mechanical design features a modular approach using eighteen double sided, plated through printed circuit boards housed in machined, *irradiated* aluminum assemblies. That text should have said that the circuit boards are housed in machined, *irridated* aluminum assemblies. Irridation is a chemical process by which the aluminum is etched to give it a frosty, textured surface that is fingerprint resistant.

In Part 2, an incorrect photo swap occurred after the issue went to the printer. The lead photo for Part 2 was intended to be a view inside the radio with the top cover removed. Instead, that photo shows a view inside the radio with the bottom cover removed. The caption does not describe what you see in the photo. (The correct photo — and caption — appear in the version of the article posted to the *QEX* Web site at **www.arrl.org/qex/2008/03/Drentea.pdf**. The correct photo is also reproduced here as Photo A. Visible from the left are the FSYNTH assembly (left side panel), the IF75BC assembly (top left), the automatically switched half-octave receiver band-pass and transmitter high power, low-pass filter bank assembly, and the DFCB command and control assembly and keypad mounted on the back of the front panel. Front panel, side panels, top and bottom are removable, allowing access to the assemblies.

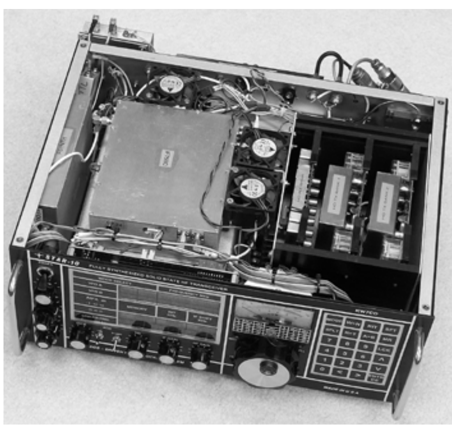


Photo A

On page 33 of Part 2, near the top of the center column the text says "The synthesizer in Star-10 goes a step further by generating the LO frequencies at ten times the required frequency range, or 770 MHz to 1050 MHz for improved phase noise performance after a division by 10, which facilitates a 6 dB improvement at the divided down 77 MHz to 105 MHz." The improvement in phase noise performance is 20 dB, not 6 dB—*Ed*.

Introduction

In Part 1 of this series, I presented a system design criteria for a modern double conversion transceiver, namely the *Star-10*. [Part 1 appeared in the Nov/Dec 2007 issue of *QEX*. That issue is currently out of print, but the *Star-10* article was the sample article from that issue. It is available on the *QEX* Web site at: **www.arrl.org/qex/2007/11/drent.pdf**. — *Ed*.] A complete discussion of how the transceiver works was also presented along with an introduction to the technologies used in the transceiver development. Also, in Part 1, I presented a set of predicted and actual performance specification numbers for the developed transceiver. A block diagram of the entire system was introduced in Figure 2 and ample composite dynamic range and system spurious analysis were presented in Figures 3 A, B, C and 4 A and B. In Part 2 of this series, I discussed in detail, the design and development of several major assemblies for the *Star-10* transceiver, particularly the IF75BC, BILAT AMP, FL75, FSYNTH, MRU, Half Octave Filter Banks, IF9BC, DFCB and the IF9RX. [Part 2 of this series was published in the Mar/Apr 2008 issue of *QEX*. That part of the article is also available on the *QEX* Web site at: **www.arrl.org/qex/2008/03/Drentea.pdf** — *Ed.*] I will next discuss the remaining assemblies, along with final thoughts regarding their development, key performance results and lessons learned from the entire project experience.

Product Detector Audio Frequency Assembly (PDAF)

Referring to Figure 2 from Part 1, the PDAF assembly provides final receiver conversion to audio frequencies of the detected signals after they have been filtered and conditioned (AGCed) for final detection in all modes of operation. A properly shifted BFO signal is provided from FSYNTH depending on the mode being used and commanded through the DFCB assembly. The PDAF assembly contains a high-level product detector using a class II mixer, a BFO buffer amplifier (another CA2832) providing injection to both the product detector and the transmitter mixer in IF9TX. An audio amplifier follows the product detector. In addition to audio amplification, it provides audio mixing functions in order to integrate audio feedback signals from the microprocessor as well as the CW side tone signals. A schematic diagram of the PDAF assembly is shown in Figure 27. The actual PDAF assembly implementation is shown in Figure 28.

Looking at Figure 27, the BFO signal coming from FSYNTH enters the PDAF assembly at J1. It is immediately amplified by the class A amplifier, U1, another CA2832 unit. This amplified BFO signal is further split by A1, which is a Mini-Circuits PSC2-1 part. Half the signal is passed on to J3, which distributes it to the transmitter mixer on IF9TX. The other half goes through a pad made of R4, R5 and R6 and is input to MIX 1, a high-level class II, SRA-1H mixer that serves as the product detector. This mixer was purposely selected for this function, as it is suitable for baseband frequency response output, compatible with audio frequencies, and has a reported IP3 of +28 dBm.

The conditioned 9 MHz IF receiver signal coming from IF9RX is input to the product detector mixer at J2. The mixed down audio product is matched and filtered via L1, C4, R7, R8, C5, L2 and C6, and is further processed by Q1 and U2 to be finally presented to U3, a TDA2003 audio block and output at J4-B. The L2, C5 and C6 audio low-pass filter is intended to suppress noise beyond 3 kHz. Tones from the CW side tone generator along with various feedback tones coming from the DFCB command and control

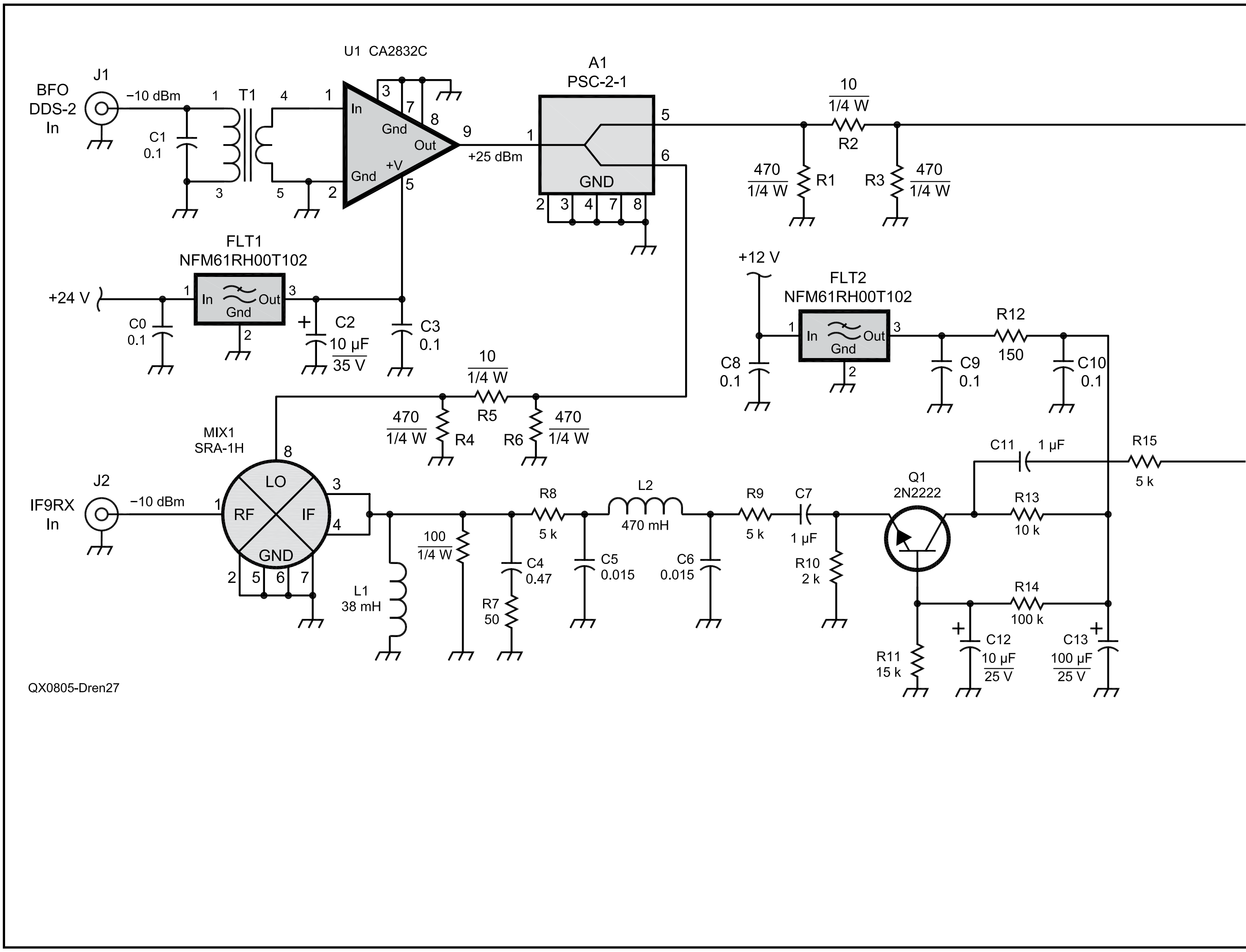


Figure 27 — Schematic diagram of the product detector audio frequency (PDAF) assembly.

assembly are audio-mixed and injected in this circuit via the J4-A connector as shown. In addition, volume control wires from the front panel audio control are input via this connector along with the MUTE signal from the T/R assembly, which silences the receiver via Q2 when transmitting.

Digital Signal Processing

Digital signal processing (DSP) can be implemented with the *Star-10* at baseband audio frequencies as shown in Figure 2 of Part 1. This can add further refinement to the transceiver's performance.

For DSP, I used the Silicon Pixels 16-bit DMA — Chroma SOUND, Audio DSP software, V 0.19 (**barberdsp.com/**). This requires the addition of a PC with a full duplex 16 bit sound card with the software installed.

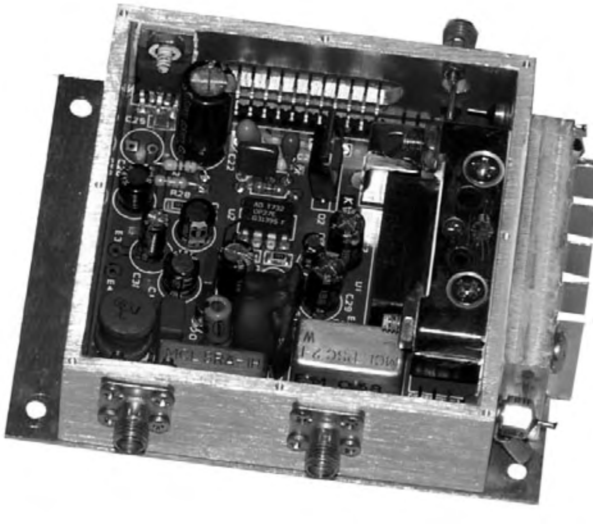
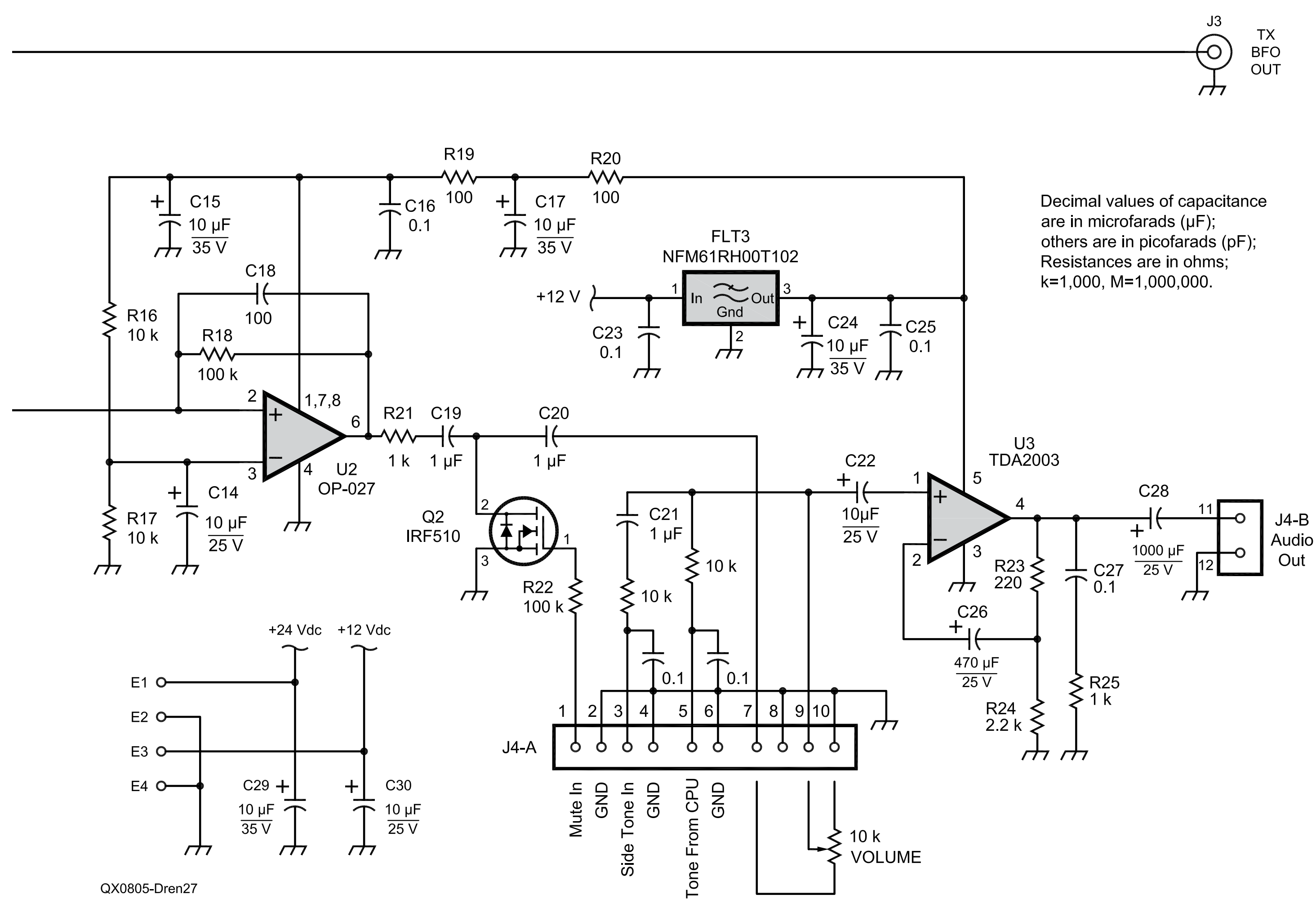


Figure 28 — This photo shows the implementation of the PDAF assembly. Visible at the right is the class A amplifier (another CA2832), which buffers the BFO signals for both, the receiver product detector mixer, as well as the transmitter mixer. The product detector is a high level class II mixer (SRA-1H), which is visible at the bottom right. The audio amplifier chip (TDA2003) is visible at the top left side of the assembly. Various other circuits are also visible.



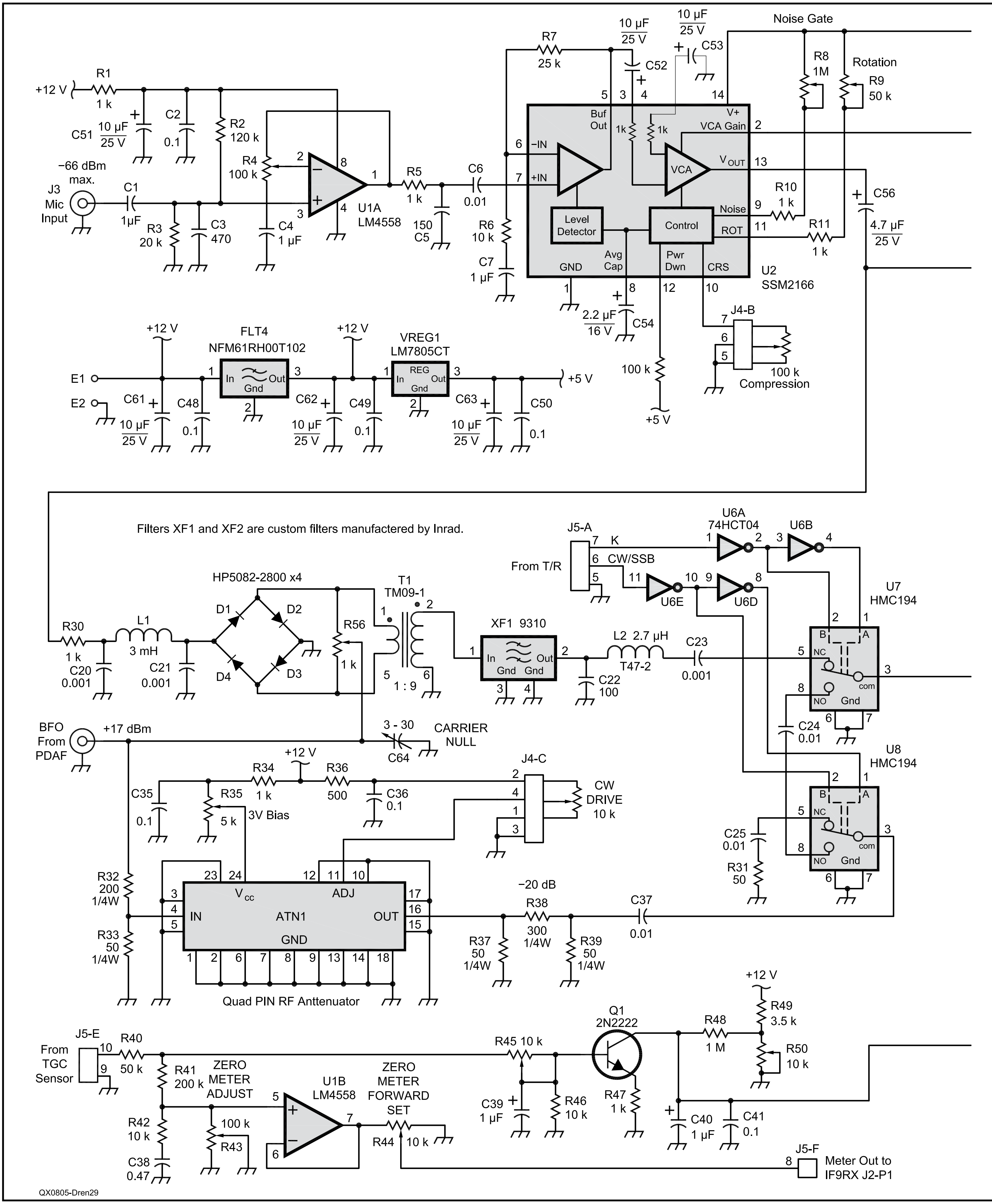
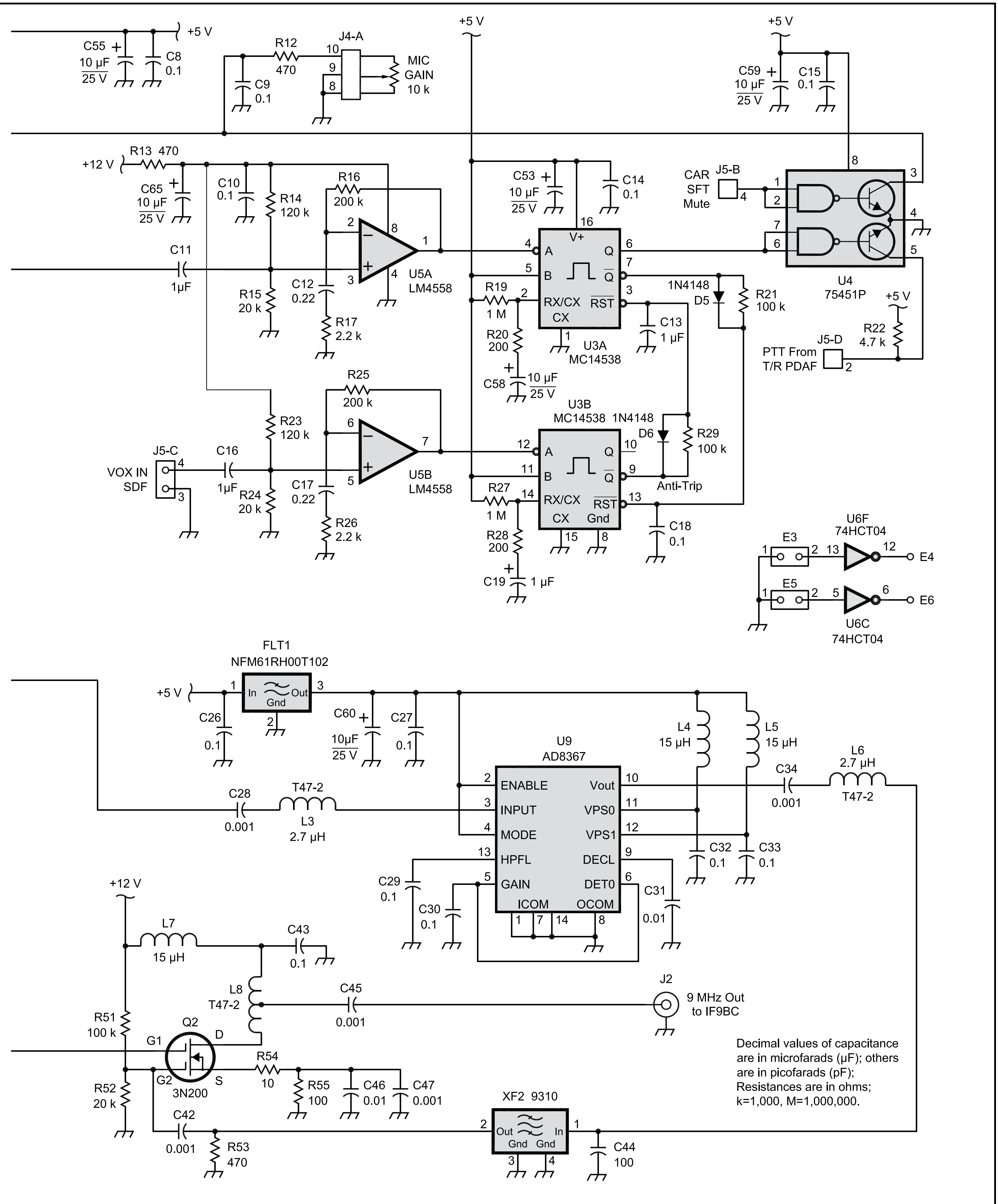


Figure 29 — Schematic diagram of the IF9TX assembly. IF9TX performs all key transmitting functions as commanded by DFCB and using the BFO signals from the FRU — FSYNTH.



Decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); Resistances are in ohms; k=1,000, M=1,000,000.

This excellent software is intended for *Windows 95/98/NT/2000/XP* and can provide a lot of additional functionality for the transceiver. Among the functions are: Noise reduction of SSB signals, automatic notch filtering for removing tones, band pass, low pass, high pass, and band stop (manual notch) filters. Filters can be user-defined, using the built-in graphical filter designer. Additional functions can be selected. Among them are pre-defined filters. One can just drag a filter from the design window to an empty button, and a new filter bandwidth can be designed into the menu. In addition, an AGC function can be selected. Since there is no such thing as a perfect AGC circuit, this can temper possible shortcomings in the previous analog AGC circuits of the transceiver under varying conditions.

The Chroma SOUND software addition further improves the already outstanding performance of the *Star-10,* which benefits from good image rejection due to the transceiver's high first up-convert IF, and a well behaved RF/IF signal processor, using up to 32 poles of cascaded quartz filters.

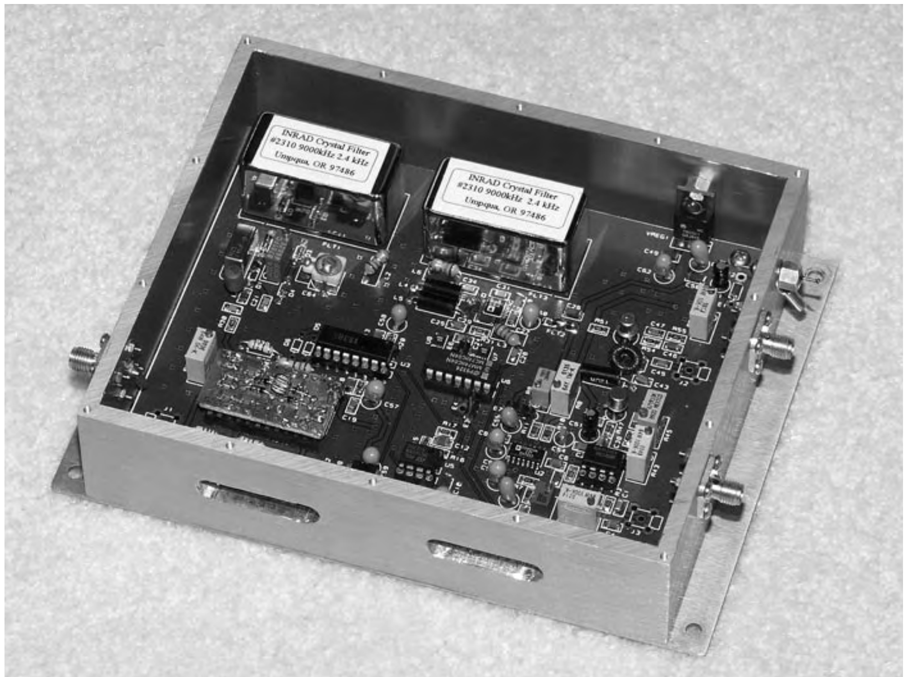


Figure 30 — Actual implementation of the IF9TX assembly. Visible at the top are the two cascaded 9 MHz, 2.4 kHz wide, Quartz crystal filters, which are similar to those, used in IF9RX. Another BIPA-like circuit (bottom left) is used as the CW drive control.

9 MHz Transmitter IF (IF9TX)

I will next discuss the design of the transmitter IF (IF9TX). Referring to Figure 2 from Part 1, the transmitter IF, IF9TX, performs all key transmitting functions as commanded by DFCB, using the BFO signals from the FRU — FSYNTH as buffered through PDAF. A microphone amplifier combined with a compression function and a VOX/ANTI-VOX function; condition the voice signals coming from the microphone. These signals are then input to a high level class II mixer, which in this case is made from individual components (unlike all other mixers in the system) in order to be able to control its balance. Carrier re-insertion and drive control are achieved in CW via the solid-state Hittite RF switches and another BIPA-like circuit used at 9 MHz in this application.

Transmitter gain control (TGC) is achieved automatically via a control loop fed from the TGC sensory assembly located at the back of the transceiver. This double RF sensor also provides RF power readings to the S-meter/RF Power meter via the T/R switching meter circuits located on the IF9RX assembly. There are two, eight pole — 9 MHz, 2.4 kHz wide — quartz SSB transmit filters cascaded in IF9TX, for a total of 16 poles of transmitted SSB selectivity. These filters are similar to the 2.4 KHz wide SSB filters used in the IF9RX assembly. The 16 poles were intended to keep the transmitted SSB signals within specific voice and intelligibility communications standards and not spread the information into adjacent channels. The resulting SSB signals sound crisp on the air with an audio response of 300 Hz to 2700 Hz. The schematic diagram of IF9TX is shown in Figure 29 and the actual implementation of the IF9TX assembly is shown in Figure 30.

Looking at Figure 29, the microphone audio input enters the conditioning circuits at J3. The signals are amplified by U1A and are further compressed and conditioned via U2, an Analog Devices SSM 2166 chip.[1] This professional grade audio conditioner gives outstanding performance and control over the speech waveforms with very low noise and total harmonic distortion (typically 0.25%). It offers variable compression (set at 2:1 in maximum mode) and automatic noise gating to improve the intelligibility of the microphone signals by recognizing and compensating for various signal level conditions. This circuit also uses a "downward expansion" technique (noise gate), which allows smoothing out speech transitions between words while canceling out background noise for improved signal-to-noise performance. For DX work, this "wonder chip" provides gain that is dynamically adjusted by a control loop to maintain a given set of compression characteristics. This allows using more compression when necessary, to increase average power. A high degree of flexibility was built into this chip by providing programmable VCA (voltage controlled amplifier) features, rotation point and noise gate adjustments.

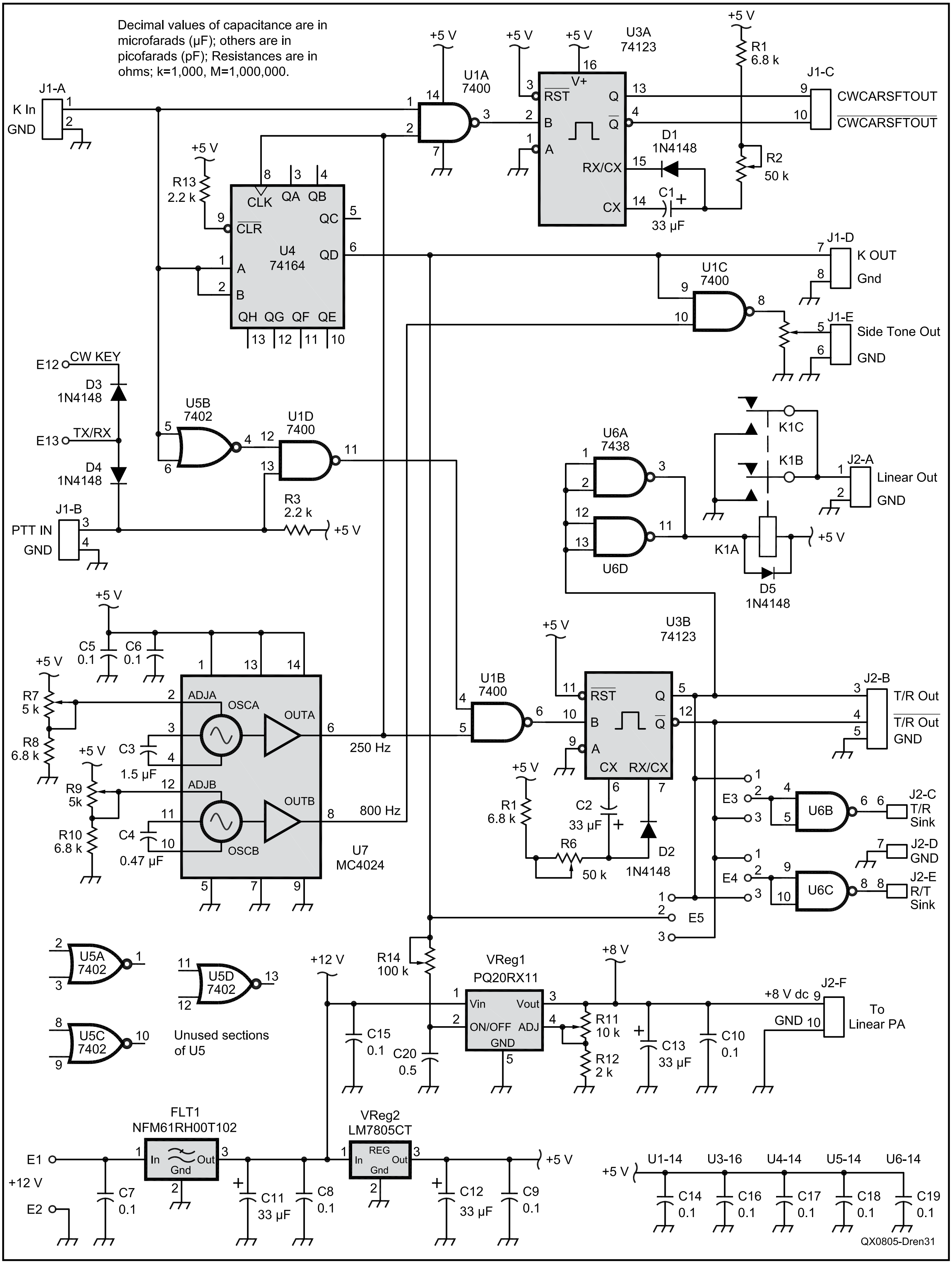
[1]Notes appear on page 49.

Looking at Figure 29, microphone gain is achieved from the front panel via J4-A. Compression level is also controlled from the front panel via J4-B. The actual controls are implemented via two concentric 10 kΩ potentiometers located on the left side on the front panel. The VOX/ANTI-VOX circuits are implemented via U5A and U3A andU3 B.

The conditioned microphone signal leaving the SSM 2166 variable compressor/noise gating device is input to a high level mixer via R30 and a low pass filter formed by L1, C20 and C21. The mixer is constructed of four matched HP 5082-2800 Schottky diodes.

Mixer balance is achieved via the combination of R56 and C64, which also serves as the BFO injection point for the various BFO frequencies (dependent on mode) selected from PDAF and coming from the FSYNTH via the PDAF assembly. It is at this point that the CW carrier is reinserted via the adjustable Quad PIN attenuator (Pi) ATN1 which is an exact replica of the BIPA circuit previously discussed in Part 2 of this series. CW drive

Figure 31 — Circuit diagram of the T/R control assembly. Various delays and commands are generated via one-shot logic circuits. A shift register (74164) is used to slightly delay the Morse code signals in order to allow the FRU — FSYNTH — to settle and lock-up between characters or character elements when switching between RX and TX and operating split. A dual clock (MC 4024) is used in conjunction with the shift register to generate the delayed Morse code characters as well as a keyed side tone signals.


Decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); Resistances are in ohms; k=1,000, M=1,000,000.
J1-A
K In
GND
U1A 7400
U3A 74123
J1-C
CWCARSFTOUT
R1 6.8 k
R2 50 k
D1 1N4148
C1 33 µF
R13 2.2 k
U4 74164
J1-D
K OUT
U1C 7400
J1-E
Side Tone Out
E12 CW KEY
D3 1N4148
E13 TX/RX
D4 1N4148
U5B 7402
U1D 7400
J1-B
PTT IN
R3 2.2 k
U6A 7438
U6D
K1C
K1B
K1A
J2-A
Linear Out
D5 1N4148
U3B 74123
C5 0.1
C6 0.1
R7 5 k
R8 6.8 k
C3 1.5 µF
R9 5k
R10 6.8 k
C4 0.47 µF
U7 MC4024
250 Hz
800 Hz
U1B 7400
J2-B
T/R Out
R1 6.8 k
C2 33 µF
R6 50 k
D2 1N4148
E3
E4
E5
U6B
U6C
J2-C T/R Sink
J2-D GND
J2-E R/T Sink
U5A 7402
U5D 7402
U5C 7402
Unused sections of U5
R14 100 k
VReg1 PQ20RX11
R11 10 k
R12 2 k
C13 33 µF
C10 0.1
C15 0.1
C20 0.5
J2-F
+8 V dc
To Linear PA
FLT1 NFM61RH00T102
VReg2 LM7805CT
E1
+12 V
E2
C7 0.1
C11 33 µF
C8 0.1
C12 33 µF
C9 0.1
U1-14 U3-16 U4-14 U5-14 U6-14
C14 0.1
C16 0.1
C17 0.1
C18 0.1
C19 0.1
QX0805-Dren31

control is achieved from the front panel via J4-C as shown. Switching between SSB/AFSK and CW operation is achieved from the T/R assembly (and from PDAF) via J5-A and through the double RF solid-state switch arrangement at U7 and U8.

In either of the single sideband modes (upper or lower), the BFO is shifted accordingly and the 9 MHz SSB transmitter path coming from the mixer follows via T1, a TMO9-1 Mini-Circuits part and enters the first quartz filter XF1 (2.4 kHz) to go through the U7 solid state RF switch to be further amplified by U9 through the second quartz filter XF2 (2.4 kHz) and is finally output to IF9BC at J2. The transmitter gain control (TGC) (otherwise known as ALC) signals coming from the RF sensor assembly located on the transceiver's back (see leading picture) enter the IF9TX assembly at J5-E. The feedback signal is processed through Q1 (2N2222) and Q2 (a 3N200), which put the brakes on the IF/RF output coming out of XF2 at J2, always limiting the RF output of the transmitter to 100 W average.

When the transmitter is operating in the CW mode, the U7 and U8 solid state switches (Hittite HMC194) change the RF path from the SSB mode to insert the BFO signal directly into this path as controlled from the ATN1 CW drive and to be conducted through the U9 and XF2 path, through the TGC control circuits and to be output at the same J2.

Additional muting circuits are implemented via the T/R Switching Director assembly shown in Figure 2 of Part 1. DC power for the IF9TX is supplied as on any of the other *Star-10* assemblies, through on board tubular filters and regulators, as shown.

The IF9TX assembly is as unique as the IF9RX assembly. It accomplishes several transmit functions as commanded from the command and control assembly, DFCB assembly, the FSYNTH and the PDAF assemblies.

Transmit / Receive (T/R) Controller

The T/R control assembly in the *Star-10* is implemented using an all-digital approach. It operates in conjunction with the DFCB assembly, the IF9TX assembly, and the T/R Switching Director assembly. It accomplishes all T/R functions as shown in Figure 2 of Part 1.

The T/R assembly receives commands from the push-to-talk circuits, the VOX circuits and the CW key commands. Some of its functionality is also routed through the microprocessor in the command and control DFCB assembly. The T/R assembly outputs several control signals including the carrier shift commands in CW, the T/R control signals for closing the on-board high power linear amplifier switch-over relay circuit, the MUTE commands for IF9RX, PDAF and the Switching Director assemblies. In addition, it produces an 8 V dc bias control voltage to the power linear amplifier.

The T/R assembly is equipped with a dual square wave oscillator circuit (MC 4024), half of which provides keyed side tone audio signals to the audio mixer amplifier circuits in PDAF, the other half serves as a clock for a Morse code character shift register intended to delay slightly the code to the keying circuits on the IF9TX in order to allow the FRU — FSYNTH — to steer and lock-up between received and a transmitted frequencies when operating split and/or even between code characters when switching back and forth between the two split frequencies. The T/R control assembly is shown in Figure 31.

Looking at Figure 31, the PTT and/or Key functions are ORed together via the J1-A, E12, E13 and J1-B inputs. The signals are combined through the debouncing functions on DFCB as we previously discussed. A series of events are created upon key down or PTT, depending on the mode selected from DFCB.

In CW, the keyed signals are slightly delayed by a few milliseconds through the shift register at U4 (a 74164 shift register) and output through J1-D to be presented further to the IF9TX keying circuits. This delay is necessary to allow the synthesizer to settle down before shifting out the first CW character elements when working split between two different RX and TX frequencies. The delay is created in U4 as clocked by the 250 Hz oscillator A, at U7 (MC 4024). This short delay does not affect the operator perception of the transmitted CW keying. The 800 Hz side tone oscillator is implemented similarly at oscillator B of U7 (MC 4024). It is gated together with the delayed keyed Morse code and is output to the PDAF audio mixing circuits at J1-E.

Carrier shift commands are started through the logic circuit U3A, one half of a 74123 one shot. This one-shot circuit delays the release time of the shift commands briefly. The carrier shift command is output at J1-C. T/R commands are output through J2-A. These commands are intended for the external power linear amplifier switch over relay keying. Additional T/R control signals are output at J2-B and J2-C. The keyed regulated 8 V dc bias for the transceiver RF linear amplifier circuits is output via J2-F. This completes the T/R assembly description.

Power Linear Amplifier (PA)

The power linear amplifier for the *Star-10* is an adaptation of an off-the-shelf 100 W plus RF power brick available commercially. An initial amplifier was designed and developed following the Motorola application notes. This approach was abandoned later in favor of the current design because of parts availability. The power amplifier assembly is shown in Figure 32 A. The assembly has been mounted on a massive heath sink including the two fans visible in the back of the assembly as shown in Figure 32 B and C.

Looking at Figure 2 from Part 1, the transmitted signals are converted to the HF range by the H-mode mixer on IF75BC. The signals are further low pass filtered and amplified by the on-board class A amplifier (another CA2832 monolithic amplifier). This output is further presented to the power linear amplifier as shown.

The design of the RF power amplifier block is typical of 13.7 V power amplifier design. The first stage in this amplifier is operated in class A. Frequency response is compensated with feedback via a capacitor in parallel with the first transistor emitter resistor. Then the signal is amplified further by a low power push-pull amplifier. The output of this low power amplifier is coupled to the high power final push-pull amplifier stage. Additional feedback circuits are used throughout to keep gain relatively flat over the entire HF range. Cooling control is achieved by sensing temperature changes via an on-board thermistor, and using comparators, which activate the two fans when temperature exceeds 100°F. Higher fan speeds can also be achieved automatically. The output of the power linear amplifier is then passed to the half octave low-pass filter banks as previously discussed. From there, the RF signals go through the sensory electronics (see Figure 32C left), which in turn, feed the TGC circuits on IF9TX as previously discussed.

Other Assemblies (IF9NB)

Among the other assemblies in the *Star-10* are the Switching Director assembly, which provides additional muting circuits for the IF9BC, and the wide band IF amplifier and noise blanker assembly — IF9NB — as previously discussed in Part 1. This assembly provides wide spectrum analysis functions at 9 MHz, noise blanker detector functions to be fed to the BIPA circuit in IF9BC, and an oscilloscope function via a fixed conversion to 455 kHz.

Looking at Figure 2 from Part 1, the IF9NB assembly uses the 500 kHz wide IF signals from IF9BC. It amplifies them and triggers the one shot blanking circuits, which in turn blank the receiver through BIPA in IF9BC. The schematic diagram for IF9NB is shown in Figure 33.

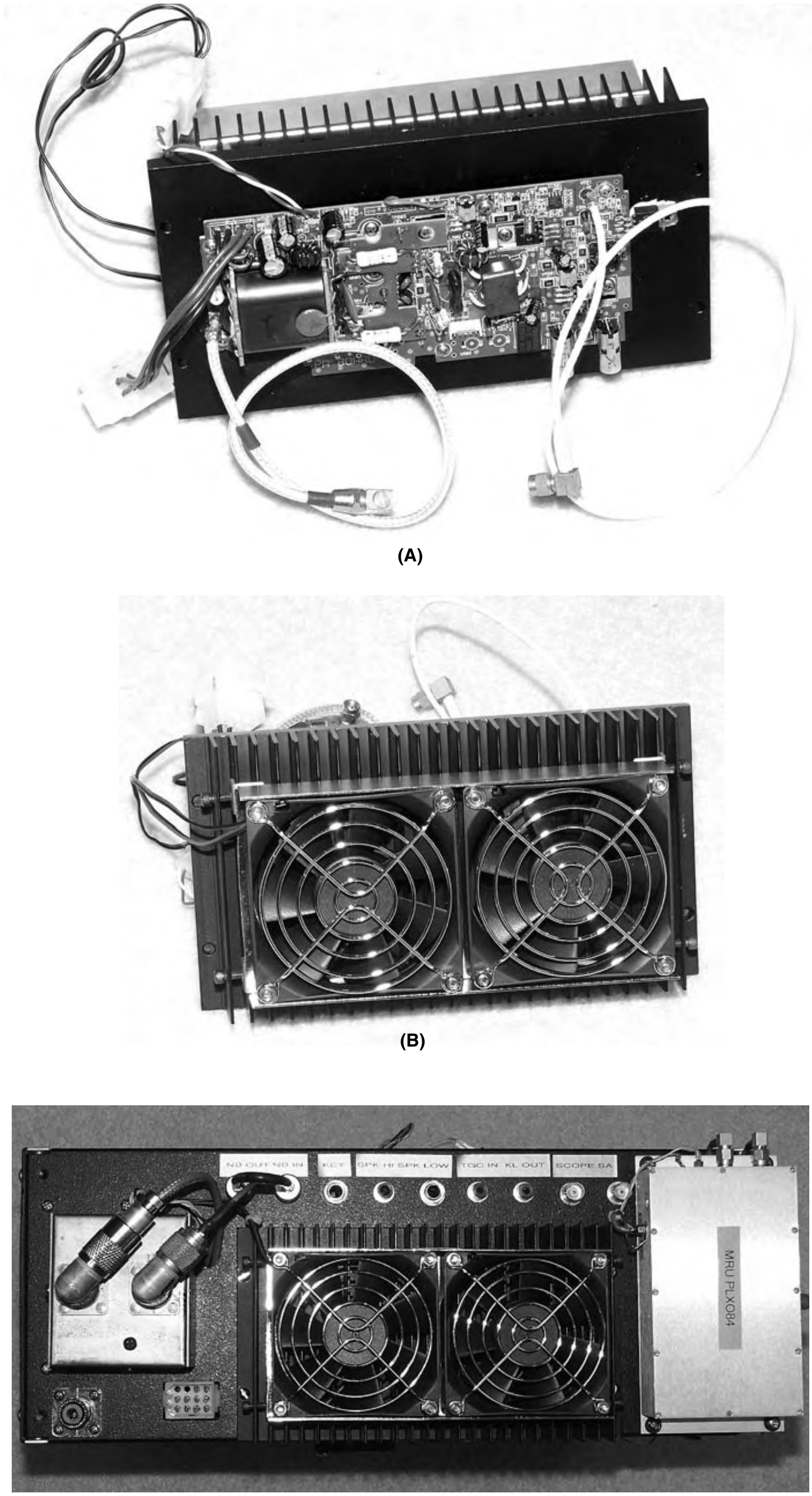
Looking at Figure 33, the 9 MHz wide IF signal (500 kHz) from IF9BC enters at J1. It is amplified and AGCed by the AD8367 amplifier at U1. From here, the wide signals are fed to the 2N2222 amplifier and the squaring circuits at Q1 and Q2. Another part of the signal is fed through a second path to a CP643 amplifier, Q3, to be output to an external spectrum analyzer with a 500 kHz bandwidth for viewing band activity at J2. To facilitate the spectrum analysis display function of the IF9NB, a modified SoftRock-40 SDR board was tested by KG6NK in a fixed 9 MHz receiver configuration, together with pertinent software and a PC equipped with a 16 bit audio card. This worked quite well over a displayed bandwidth of 20 kHz. The 16 bit card limited the dynamic range displayed. A 24 bit audio card would probably have given better results, but it was not tested.

The noise blanking function works as follows. The clipped signals (by CR1) from Q2 trigger one half of an adjustable pulse width one-shot, 74HCT123 at U2A. Pulsed blanking signals are output to BIPA via J5. Pulse width control is achieved from the front panel via the J5 connector as shown. A separate 9 MHz IF narrow signal coming from IF9RX is fed to the assembly via J3. It is converted to 455 kHz via a simple NE602 converter at U3. The on-chip local oscillator is a fixed quartz crystal, X1, oscillating at 8.545 MHz. The 455 kHz IF output is filtered via a 3 kHz wide Murata ceramic filter and is further amplified by a MAR-7 amplifier at U4. The oscilloscope signals are output at J4. This circuit is still being tested. This completes the IF9NB assembly description.

Switching Power Supply and Power-ON circuits

A special switching power supply (ATX-4) was built expressly for the *Star-10* by Phil Eide, KF6ZZ. The requirements called for a dual-output secondary (13.7 V dc and 24 V dc), triple EMI filtering, high speed over-voltage protection (that actually works), over-current protection, and a fast control loop to correct for anything the *Star-10* may demand. The design was derived from the ATX-1 design published in *QEX*.[2] ATX-4 is essentially the same as ATX-1. The demanding EMI control requirements, however, were imposed on the design, along with the most important design criteria, which was full protection of the expensive CA2832 amplifier blocks ($100 each) on the 24 V line.

Although beyond the scope of this article, the design of the ATX-4 has been very involved due to the radio frequency interference (RFI) requirement imposed on the power supply. Extreme EMI filtering has been used and the result has been outstanding. The ATX-4 has been used extensively



(A)

(B)

(C)

Figure 32 — Part A shows a photo of the RF power linear amplifier. B shows the cooling fans that are an integral part of the RF power linear amplifier assembly. They are mounted on the black anodized heat sink on the back of the assembly. The back of the *Star-10* transceiver is shown in Part C. The RF power linear amplifier and cooling fans are in the center. Sensory electronics are on the left and the master reference unit (MRU) is on the right.

with the *Star-10* and provides a totally clean RF environment on all bands of interest.

The ac power to the *Star-10* power supply is switched on and off from the front panel of the radio via a small power switch. This switch acts as a TTL level shifter to a solid state ac power relay (REDAC) located in a custom-made ac power strip in which the ac power cord of the power supply is inserted. The 5 V TTL voltage is derived from four AAA rechargeable batteries located under the bottom panel of the transceiver. The batteries are constantly being trickle charged by a small 6 V dc charger.

Four microprocessor cooling fans are used to cool the assemblies containing CA2832 amplifiers in the transceiver. These acoustically quiet fans use specially selected, dual-speed brushless motors that have been chosen on purpose because of their superior RFI performance. They are powered via a separate 12 V dc power supply in order to provide the greatest immunity to the receiver from RFI.

Putting it all Together

As previously mentioned, the *Star-10* final assembly has been the culmination of several years of RF design and development. It reflects modern state-of-the-art approaches to HF transceiver implementation. Its realization encompassed the many phases of engineering and development usually encountered in a complex commercial or military piece of equipment, from the system design through the circuit and software design, the multiple brass boarding, the complex testing and packaging into the final form factor as described in this series.

The *Star-10* packaging is complex and modular. All assemblies with the exception of the DFCB are enclosed in irridated machined aluminum RF enclosures available from COMPAC Corporation. These assemblies are mounted on two major shelves in the main enclosure as discussed in Part 2 of this series. These custom shielded assemblies are held together with multiple miniature flat screws, forming RF gaskets to provide better than 80 dB of isolation up to a GHz. The slots for interface connectors have been machined into the enclosures, thanks to Brendon Holt, KC5VCW. He donated his time and equip-

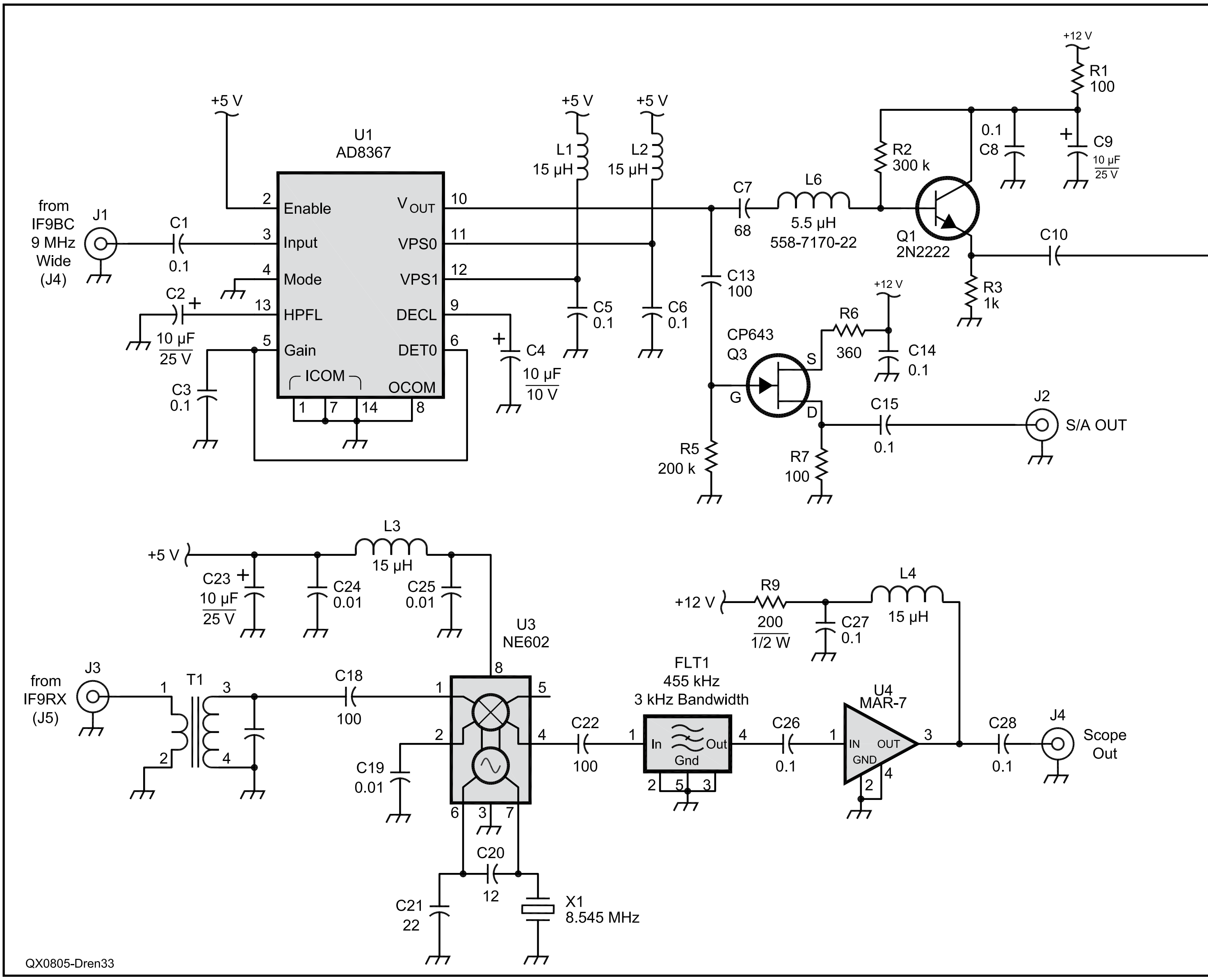


Figure 33 — Here is the schematic diagram of the IF9NB assembly. This assembly provides wide spectrum analysis functions at 9 MHz, noise blanker detector functions to be fed to the BIPA circuit in IF9BC, and an oscilloscope function through a fixed conversion to 455 kHz.

ment to the *Star-10* cause.

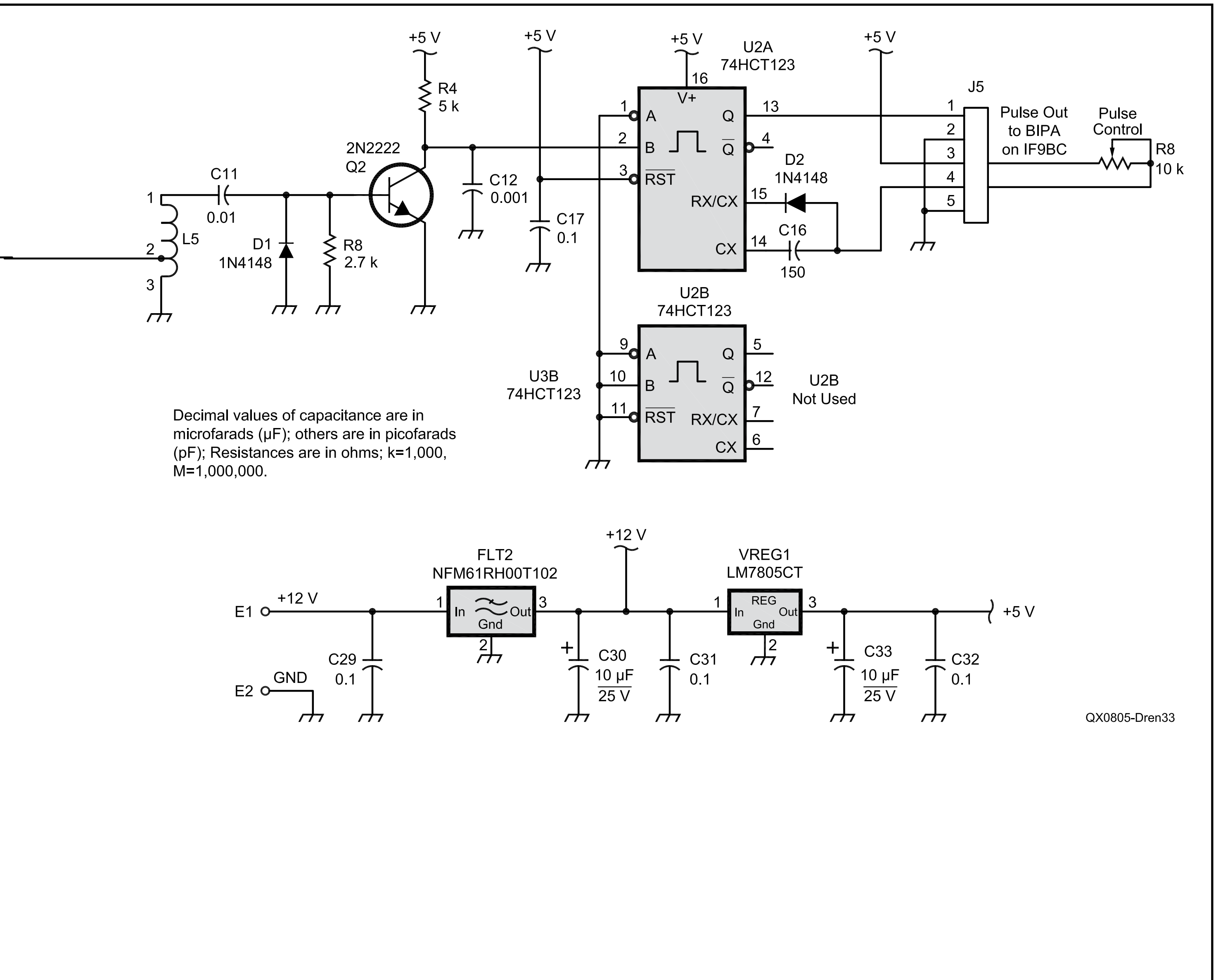
The *Star-10* circuit boards have been specially designed to install directly in the various sizes of machined aluminum boxes. They have been laid out expressly for the boxes and have been professionally executed on G-10 double sided circuit board material with plated through holes using multiple stitched ground planes, surface mount technology (SMT), along with hybrid assemblies.

The main enclosure was manufactured using aluminum panels that were professionally bent, sand blasted, irridated and painted with hammer baked black paint except in the areas where they meet, for RF shielding contacts. This enclosure was fabricated thanks to James Moon of M&R Sheet Metal & Mfg, Inc, in Tucson, Arizona.

The front panel is made of two large black anodized aluminum plates sandwiched together. They have been machined differently with respect to each other using cut-outs to hold the DFCB and keypad assemblies behind and hide them under panel holes, using flat screws and spacers. Thick film (0.8 mm Ortho Type III) membrane dials were manufactured from scratch using precision line artwork, photomechanical negative contact techniques and a large process camera. These dials have been sandwiched between the two anodized panels as shown in the transceiver main pictures. They are transparent in some areas to show through the displays, along with areas that have been selectively painted behind with silver paint to match the white silk-screened information painted on the black anodized front panel. Thus, a black and silver/white composite front panel resulted. I think this has a very "clean" look.

The *Star-10* assembly and testing came to full fruition during a three-week-long period in a well-equipped laboratory, courtesy of KG6NK, as shown in Figure 34. It should be noted that without the right testing tools, such a project could have not been completed. Although very intense, the final assembly went together without any major problems. There were no showstoppers.

Although the packaging was very tight, the radio performed as designed. As with any new design of this magnitude, slight changes had to be incorporated in some of the circuits and the inter-assembly interfaces during the



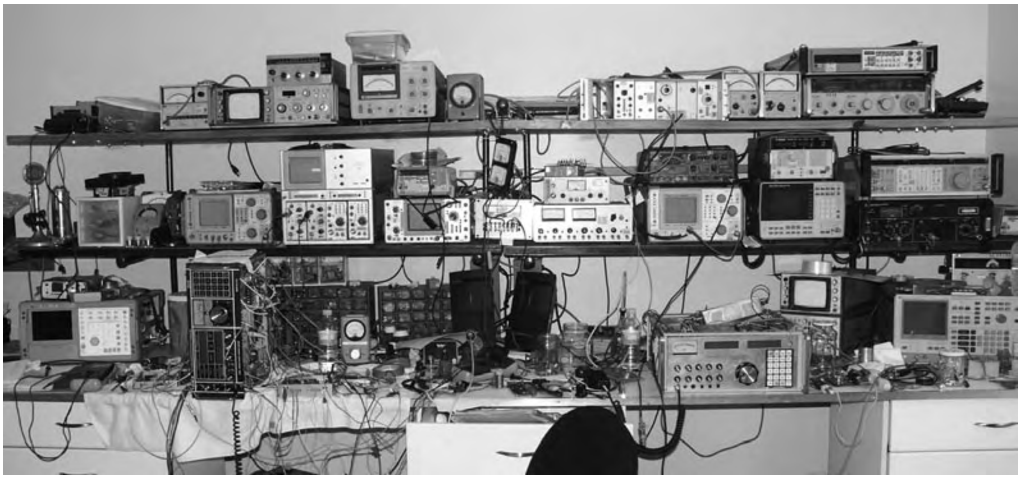


Figure 34 — The well-equipped KG6NK laboratory was used to complete the final wiring and testing of the *Star-10* transceiver. KG6NK's indisputable troubleshooting skills proved invaluable in the design, assembly, testing and especially in the final stages of the implementation.

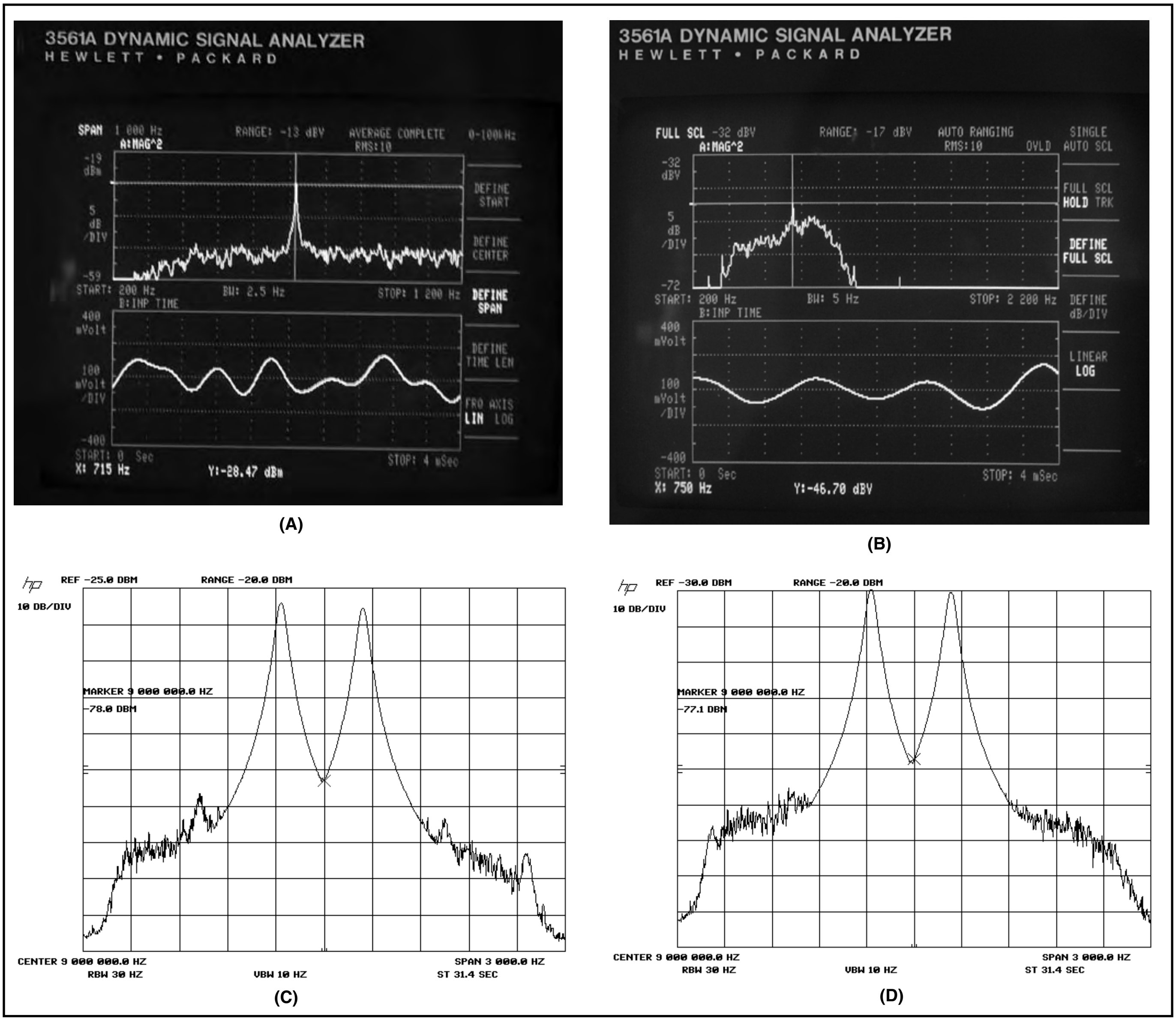


Figure 35 — Blocking dynamic range (BDR) at 5 kHz offset using 2.4 kHz ultimate bandwidth is shown in Part A. (Note: The values are expressed in dBm.) Part B shows the blocking dynamic range (BDR) at 5 kHz offset using 500 Hz ultimate bandwidth. (Note: The values are expressed in dBV.) The in band (2.4 kHz) receiver performance with two tones spaced at 500 Hz is shown in Part C. With the –15 dBm (S9+50 dB) signals applied at the receiver's input, in band spurs were 55 dB down. Part D shows the in band (2.4 kHz) receiver performance with two tones spaced at 500 Hz. With two RF signals 500 Hz from each other at –63 dBm (S9+10 dB) spurs were way down.

final assembly. These modifications have been introduced gradually until the system became stable. Most troubleshooting focused on finding and repairing pesky little contacts in silver or tin over gold connections in the signal connectors. Some of the coaxial cables have been found to be length sensitive and had to be cut to exact sizes. Several SMA type tubular, mil spec, RF attenuators have been occasionally inserted between RF assemblies. Comprehensive laboratory tests followed the final assembly.

A series of on the air tests followed. Reports from many DX stations proved that the transceiver's intelligibility in pile-ups is superior with the signal being picked up on the first or the second call despite the fierce competition. With the exception of some preliminary audio and compression level testing, crisp audio was always reported, proof of the microwave synthesizer's outstanding phase noise performance. The variable compression and noise gating features of the microphone circuits worked as designed. The receiver performance was equally good. The receiver's phenomenal IP3 spurious free dynamic range, and especially the blocking dynamic range allowed copying S1 or S2 SSB signals in the vicinity of 30 dB over S9 signals at only 3 kHz away from the desired signal. The receiver shines especially on CW during contests, when signals can be easily separated with precision at 500 Hz or less from each other by employing all 32 poles of cascaded IF filtering. Split operation was tested thoroughly as well as the RIT, pass band tuning (shift), memory, S-meter linearity, scanning and all other features.

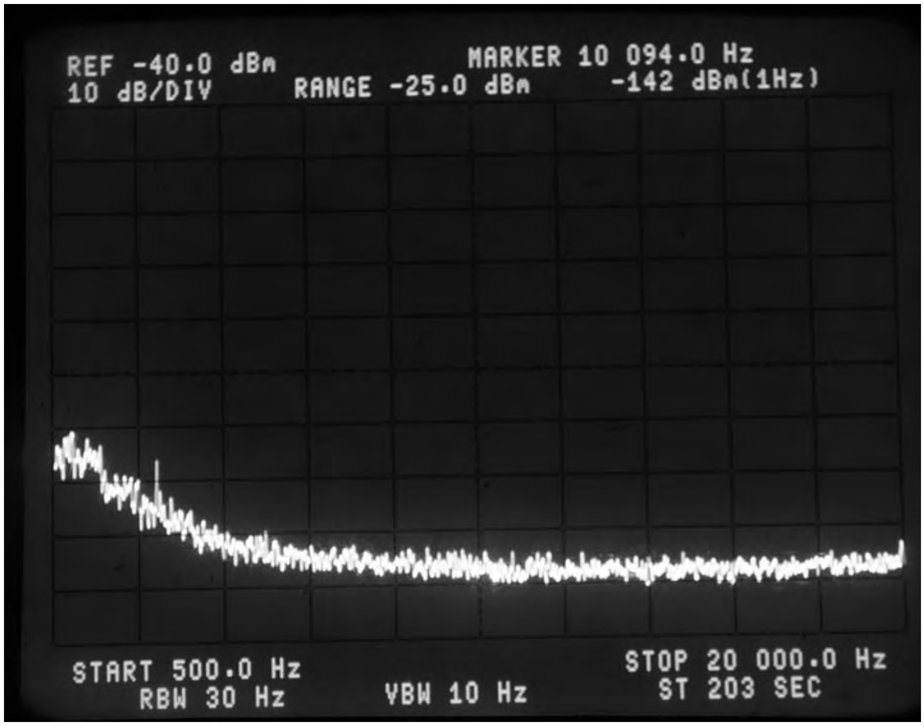


Figure 36 — The absolute phase noise measurement capability of the HP-3585A spectrum analyzer was calibrated using two HP-8640 generators in a classic mixing type phase noise measurement system. This capability was –142 dBc/Hz as shown.

Performance and Tests

Performance goals and specifications were presented in Part 1 of this article series. Comprehensive tests were performed in the laboratory. The MDS of the *Star-10* with the preamplifier ON was measured at –136 dBm in a 500 Hz ultimate bandwidth (with BIPA at zero dB). This was determined using a new calibrated Agilent E 6380A test set generator and an HP-400GL AC voltmeter and an HP-3561A . To verify accuracy of the Agilent 6380A, these numbers were also checked using a Fluke 6071A generator and a Tektronics 495P spectrum analyzer. The results were similar. This MDS is in line with predictions from Part 1 and is comparable with results obtained from a modified FT-1000D with the preamplifier ON. A test against the IC-7800 was also performed.

The 1 dB compression point of the FT-1000D with the preamplifier ON was found at –10 dBm. The 1 dB compression point of the *Star-10* receiver with the preamplifier ON and without the AIPA and or BIPA attenuators activated was found to be 0 dBm

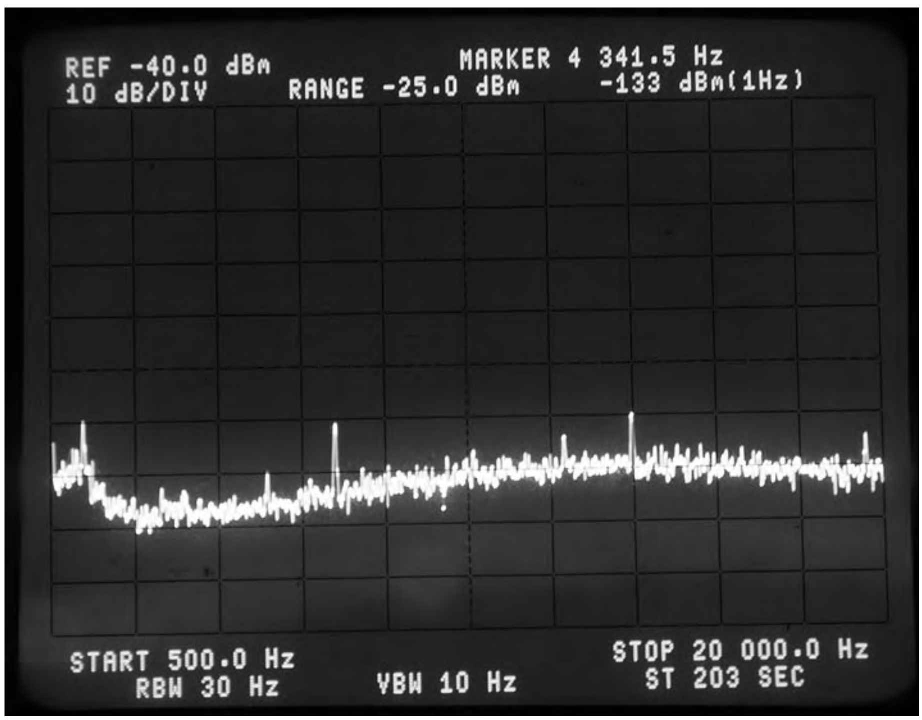


Figure 37 — Close-in phase noise performance of the FRU — FSYNTH — at 89.2 MHz (14.2 MHz) is –133 dBc/Hz. Phase noise performance has been tested and found to be uniform (within 1 dB) over the entire frequency coverage. The little spikes are spurs from the DDS, which are inside the loop filter, and cannot be eliminated. They are typically –100 dBc. These low spurs have not been audible in tests. See text.

(10 dB better). With AIPA and BIPA applied, the 1 dB compression point of the *Star-10* was found to be greater than +30 dBm. The receiver's composite linear dynamic range was found to be greater than 150 dB (500 Hz bandwidth, and all AGCs (AIPA + BIPA) turned on). This performance was listed in Part 1. The receiver's IP3SFDR was at least 130 dB using 20 kHz tone spacing (using a KW7CD test set with two combined quartz generators at 14.020 MHz and 14.040 MHz) and a 500 Hz bandwidth with the preamplifier on, and the AGC on. The *Star-10* receiver IIP3 was found at +45 dBm with the preamplifier on, just as predicted in Part 1.

The most demanding kind of dynamic range is, of course, the blocking dynamic range (BDR). *Star-10* receiver's blocking dynamic range (BDR) is due to an extremely crunch proof front-end design, the use of high-level mixers throughout, the superior microwave synthesizer used, and the superlative 32 poles of cascaded IF filters.

The *Star-10* blocking dynamic range was tested at 14.200 MHz using an HP-3561A dynamic signal analyzer as shown in Figure 35 A and B.

It was found that that with a –20 dBm interfering signal (the equivalent of an S9+ 53 dB signal) offset by only 5 kHz from the received frequency, the *Star-10* receiver can discern a –110 dBm signal (the equivalent of an S1 signal) with a 20 dB SNR when using the 500 Hz ultimate BW filter, with the preamplifier ON, no attenuators applied and no AGC action. The interfering signal level was then brought up to –8 dBm and even to 0 dBm before the –110 dBm desired signal at 5 kHz offset was finally blocked. This kind of interference is almost never encountered in real life, but the superior performance is very evident during contests and especially in the CW mode. The effect is very audible when tuning across a very busy band with signals bursting out of the MDS, and with little or no presence of nearby signals, a phenomenon not experienced with any other kind of transceiver I have ever tested. This radio is very quiet despite its sensitivity. As the band gets busier, the *Star-10* appears content, yet sensitive and very selective. In comparison with an IC-746 PRO or a 756-PRO that I tested against, there is no contest. These radios are just as sensitive (or even more so), but proportionally noisier than the *Star-10* when bands are busy (note: they bring the noise floor up due to IMD caused by a combination of factors including phase noise performance), while the *Star-10* pulls the signals out of the noise with ease.

Additional receiver tests were performed in the KG6NK laboratory using two in band RF signals 500 Hz from each other in the wide 2.4 kHz bandwidth. The measurements were observed at the second IF output. With two –15 dBm (S9+50 dB) signals applied at the receiver's input (in the 2.4 kHz BW) third order spurs were 55dB down. With two RF signals 500 Hz from each other at –63 dBm (S9+10 dB) spurs were way down. This is shown in Figure 35 C and D. This performance explains the superior experience observed with the *Star-10*, especially on CW during a busy contest.

The *Star-10* S-meter starts moving at an input signal level of –103 dBm (the equivalent of an S3). From this point on, the S-meter shows signals in linear dB (within 2 dB) up to an S9 + 40 dB (or –73 dBm + 40 dB = –33 dBm). Corrections for insertion loss of the various IF filters are automatically applied to the IF gain and S-meter upon filter selection, as discussed in the IF9RX section of Part 2. More AGC range could be used if applying the BIPA and AIPA controls. Automatic BIPA and AIPA control in the AGC loop(s) has not been implemented, leaving these controls in the manual mode. Using these controls has been minimal due to the outstanding dynamic range of the receiver.

The phase noise performance of the *Star-10* was measured directly at the synthesizer output using a phase-locked-loop measuring system involving a high level mixer, very linear amplifiers, filters and an HP-3585A spectrum analyzer which has the feature of reporting in dBm/Hz. The system was calibrated to display the noise directly in dBc/Hz. The offset from the carrier of interest was set from 500 Hz to 20 kHz. The instrument's capability was first verified by mixing two HP-8640 generator outputs locked to each other at 89.2 MHz (892 MHz initial FRU frequency divided by 10, or 14.2 MHz transceiver frequency). The resulting phase noise capability of the instrument is shown in Figure 36.

The FRU – FSYNTH — phase noise performance as implemented in the *Star-10* was found to be –133 dBc/Hz close-in, as shown in Figure 37. Better performance has been obtained by KG6NK in his version of the FSYNTH, as shown in Figure 38 A and C.

A –137 dBc/Hz (close-in) performance can be obtained from FSYNTH by tweaking the square wave DDS output level at the PLL phase detector input, separating ground planes between FSYNTH stages and by slightly changing the loop bandwidth. It should be noted that this performance is obtained because of the microwave frequencies used and only with a single VCO in the FSYNTH, instead of four as it is customarily done. Even better performance can be obtained with new microwave VCOs obtained from Synergy Microwave, the original manufacturer of *Star-10's* VCO. Experiments to improve on this performance are going on, with new VCOs

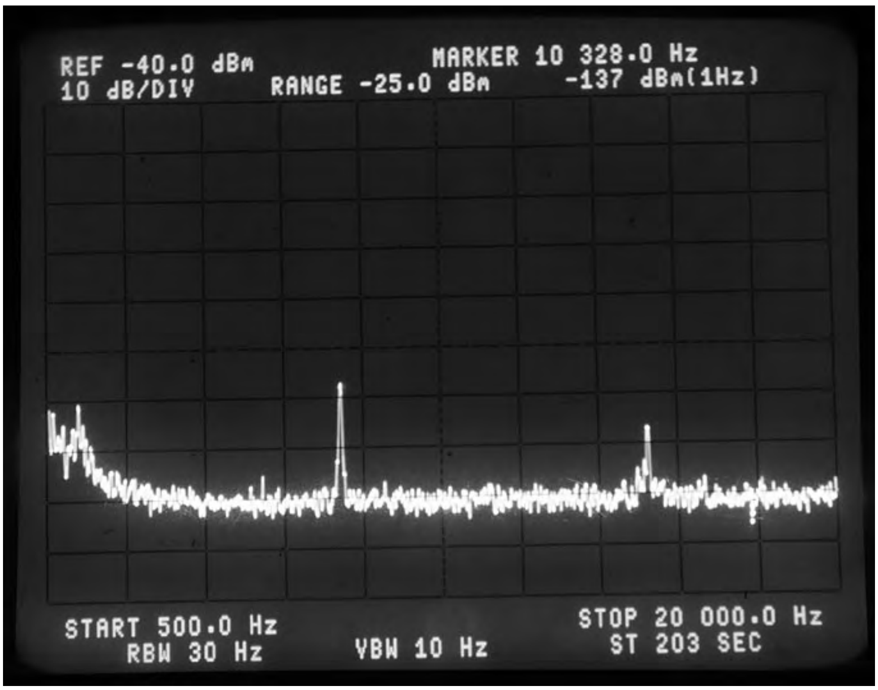


Figure 38A — KG6NK obtained –137 dBc/Hz close in phase noise performance from the FRU — FSYNTH — assembly by tweaking the circuits and widening the loop bandwidth. The previous in-band spur is –97 dBc. Listening tests proved that these spurs are not audible. Uniform performance (within 1 dB) has been obtained throughout the entire frequency range. The impact of the modifications on split operation lock-up and settling time have been analyzed and tested.

donated by Ulrich Rohde, N1UL.

The FSYNTH phase noise performance was further tested at several frequencies, 78.7 MHz (3.7 MHz), 82.1 MHz (7.1 MHz), 89.2 MHz (14.2 MHz), 96.2 MHz (21.2 MHz) and 103.4 MHz (28.4 MHz).

A final integrated phase noise plot of the FSYNTH from 10 Hz to 1 MHz offset was obtained using a PLL measuring system. The test was performed by KG6NK in his laboratory. A Bliley OCXO reference and its calibration plot against the Wentzel OCXO master was provided by John Miles, KE5FX. The FSYNTH frequency in this test was 100 MHz or 25 MHz receiver/transmitter frequency. See Figure 38B. A –138 dBc/Hz SSB phase noise was verified through this final test.

Transmitter two-tone intermodulation distortion tests were performed at 14.2 MHz with and without audio compression. The third order products were 32 dB down without compression and slightly worse with the audio compressor switched in. This is shown in Figure 38, Parts D and E. The harmonic rejection performance has been documented in detail in references 1, 2 and 3 from Part 2 of the article.

Transmitter SSB audio response measurements were performed in the upper and lower sidebands with full power (100 W) output by using an Amber 3501 audio distortion measuring system, a Bird-43 RF wattmeter and a dummy load. Although the theoretical transmitted audio frequency response was calculated to be from 300 Hz to 2700 Hz, the actual audio response under full transmit-

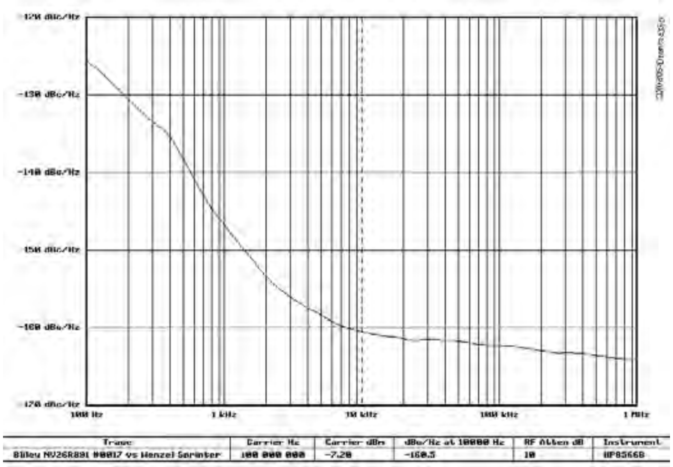


Figure 38 B — This plot shows the phase noise performance of the 100 MHz Bliley OCXO reference source used in these tests. It was calibrated against a very high quality Wentzel frequency standard. The plot shows the integrated single sideband phase noise plot from 100 Hz to 1 MHz. This calibration and plot are courtesy of John Miles, KE5FX.

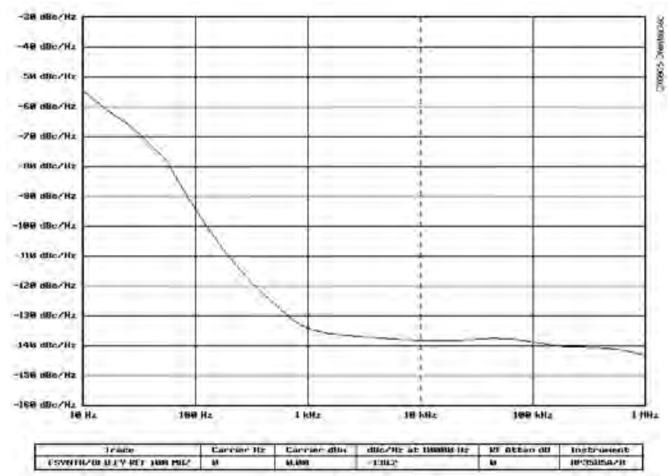


Figure 38 C — This plot shows the Integrated single sideband phase noise plot of an improved *Star-10* FSYNTH assembly from 10 Hz to 1 MHz. The performance is better than –138 dBc/Hz at 10 kHz offset. The test was performed by KG6NK in his laboratory and was obtained using a professional PLL measuring system, a Bliley OCXO reference source calibrated against a Wentzel frequency standard, and the HP-3585A spectrum analyzer. "Tool Kit PN " software was provided by John Miles, KE5FX and was implemented together with a Prologix interface, which was used to control the instrument, integrate the results, and display them. The FSYNTH frequency in this test was 100 MHz or 25 MHz receiver/transmitter frequency.

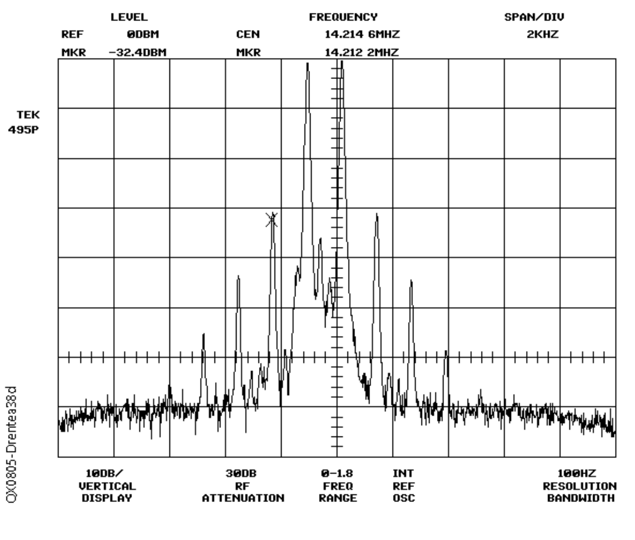


Figure 38 D — Here are the two tone transmitter test results, without compression. Third order products are 32 dB down. The tests show a clean noise floor, which is due to the FSYNTH performance.

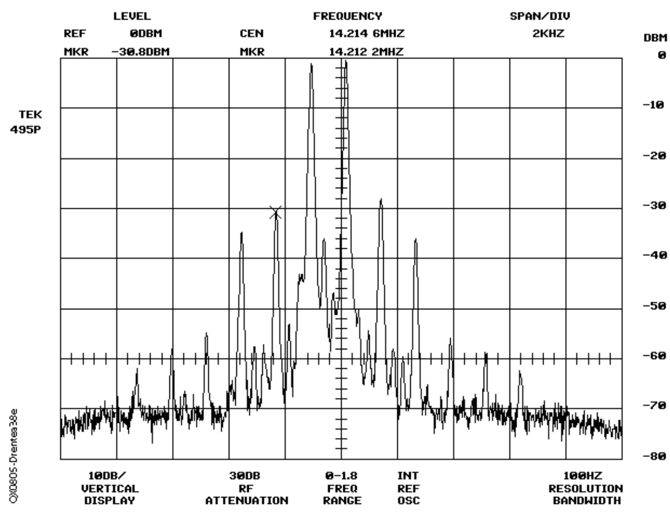


Figure 38 E — The two tone transmitter test with 2:1 audio compression turned ON is shown here.

ter output was found to be from 270 Hz to 2800 Hz at the 6 dB points. The output falls greatly before and after these points due to the 16 poles of transmit IF filtering. No splatter was ever reported from the *Star-10* during on-the-air tests. Harmonic rejection and image rejection tests have been previously performed as a function of the front-end half-octave filter banks and have not been repeated this time.

Lessons Learned

As with any new piece of equipment of this magnitude, a certain number of problems are usually expected. Because of the intense breadboarding and design verification before its final implementation, these problems have been kept to a minimum in the final version. In retrospect, most problems in the execution of *Star-10* have been mainly cold contacts in the interface control wires, connectors and relays. Some of the old relay contacts corroded and caused heating of the low pass filter banks in transmit. This situation was immediately corrected. Because of the tight *Star-10* package, access to some of these connectors has sometimes been difficult. Some problems also occurred in the SMT circuits.

After getting rid of most bugs, *Star-10* has performed reliably. Especially trouble free has been the DFCB command and control assembly and its associated software, which performed as designed after intense and careful analysis of the mathematics governing the system and operator interface. Numerous software upgrades were implemented and tested before the current trouble-free version. This combined with careful breadboarding, troubleshooting and testing the DFCB in the early phases made for an almost perfect software design. Also, the IF9TX, IF9RX and IF75BC and power linear amplifier have operated flawlessly from the start. Other assemblies required some tweaking, but have proved equally reliable after the initial hurdle.

One of the most important lessons learned from this design is that no matter how careful one is in selecting components, by the time the design is implemented, they become obsolete. Of course there is always a better way of doing things, in retrospect. This is not a new thing, however. Engineers everywhere face this kind of problem in an ever-changing industry.

A second lesson learned which goes hand in hand with the first one is to know when to stop designing circuits and not run the risk of breadboarding forever. This was hard. It required discipline and a firm gut feel about when to freeze the design.

Another good lesson learned is that no matter how careful one is in a design, things suspected to work well, don't, and things suspected to have problems might sometimes work just perfectly. This is also known as Murphy's Law.

An interesting conclusion after performing complex testing and operating the *Star-10* in rough contests is that, contrary to popular belief, roofing filters are not as important in improving dynamic range as once thought, if good front end performance is provided in the first place. As explained in Part 2, roofing filters with a 3 dB bandwidth of 10 kHz or less, that withstand the high signal levels required for ultra high dynamic range needed at this point in a system, are extremely demanding to manufacture from an IMD point of view. If the front end has the kind of performance realized in the *Star-10*, the roofing filters can be more forgiving. That is not to preclude that narrow roofing filters can greatly help overall performance of radios with lesser front-end dynamic range performance.

A final lesson learned is that no matter how good the design is; better AGCs and better noise blankers are always needed. *Star -10* makes no exception to this rule.

In operating the radio, a 500 Ω dynamic microphone with a flat response has been used. Some compression has been found useful, but not necessary, as the audio response is very crisp and distinct. Initial tests driving a full legal power linear amplifier revealed some RF feedback getting into the microphone circuits because my 20-meter beam is located right above the radio room. As any notorious RF feedback problem goes, this problem wasn't cured just with little ferrite beads and bypass capacitors as is usually found in transceiver microphone circuits. An investigation of the literature revealed not much information on RFI microphone filters.

A third order Butterworth audio low-pass filter with a 2.7 kHz cut-off frequency was designed and implemented at the transceiver microphone input, and the problem went away for good. This design was done using the AADE Filter software and is shown in Figure 39.

The *Star-10* transceiver has been in reliable operation, 24 hours a day, seven days a week for more than a year. Although three other transceivers are available here, using

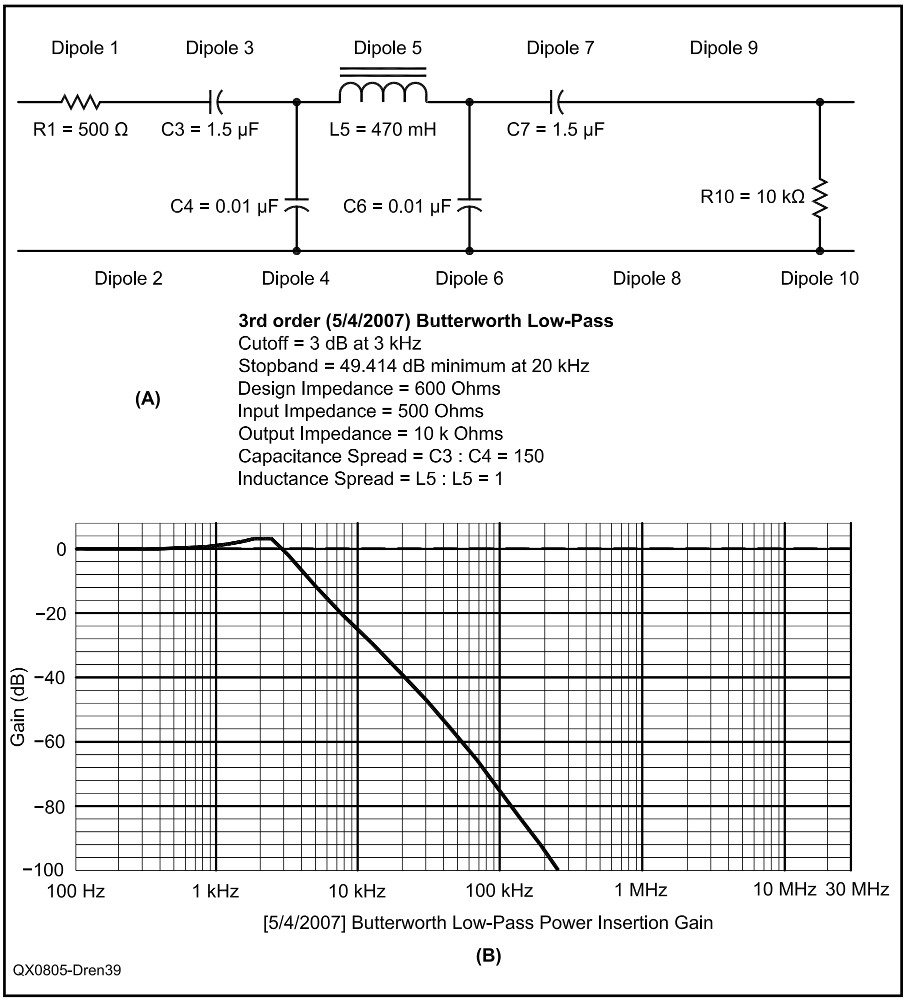


Figure 39 — Design of the third order Butterworth low-pass microphone input filter eliminates RF feedback caused by a nearby beam above the radio room when running high power.

this radio has been the preferred choice, especially when listening to busy bands. Operating this radio has been a joy due to its superior performance and its friendly user interface. *Star-10* stands ready for the upcoming, wildly predicted solar cycle.

Conclusion

The *Star-10* project has been a long and stressful engineering exercise. For the many who wrote in with their positive comments and compliments on the first two parts of the series, thank you.

This article was intended to share information. The *Star-10* transceiver was designed to prove that superior equipment can still be built and high performance combined with professional features can be designed and implemented to compete with any sophisticated transceiver on the market today. Despite this, the *Star-10* is not perfect. Even better transceivers can be built using this experience. I hope this series of articles has been an inspiration to equipment builders everywhere, to RF system designers and engineers, as well as to the armchair radio designers.

As I mentioned at the beginning of this article series, it has always been the dream of the technically inclined radio amateur to build and operate his or her own radio equipment from scratch. With a few exceptions of dedicated home brewers, it appears that operating your own home brewed radio on the bands today is a rarity. In using the *Star-10* on the air and mentioning that it is home brewed elicited some interesting reactions. Much to my surprise, comments like "Is it a kit?" or "Do they still do that?" have been commonplace.

I find this situation sad. Amateur radio used to be at the forefront of technology. Hams were the future engineers and scientists. They were persistent experimenters and innovators that achieved noteworthy technical success. It is my opinion that this trend must continue if ham radio is to remain the technical hobby it deserves to be.

It is a very proud feeling to operate equipment that you have designed and developed regardless of how simple or sophisticated it is.

Cornell Drentea, KW7CD took his first radio receiver apart (and put it back together) at the early age of six. He has been a Ham since 1957. Since then, he's built many radios and transceivers and made his passion for designing "radios" his life long profession. As an Amateur Radio operator, he is known for his extensive RF technology articles in magazines such as Ham Radio, Communications Quarterly, RF Design, *and* QEX. *Professionally, Cornell is an accomplished RF technologist, an engineer and a scientist with over 40 years of hands-on experience in the aerospace, telecommunications and electronics industry. He has been involved in the design and development of complex RF, Radar, guidance and communications systems at frequencies of up to 100 GHz. Cornell has developed several state-of-the-art RF products including ultra wide band high probability of intercept microwave receivers, complex synthesizers, multi-modulation transmitters, Doppler agile space transceivers as well as high power RF linear amplifiers. He received his formal education abroad with continuing studies and experience achieved in the United States. Cornell has presented extensively on RF design topics at technical forums such as IEEE, RF-Expo, Sensors-Expo and has given comprehensive professional postgraduate courses in RF receiver design, synthesizer design, sensors and communications. He has published over 80 professional technical papers and articles in national and international magazines. He is the author of the book,* Radio Communications Receivers, *McGraw Hill, ISBN 0-8306-2393-0 and ISBN 0-8306-1393-5, 1982 and holds five patents. He is currently available for consulting to large and small RF enterprises. You can find out more about Cornell, his consulting and his RF course offering entitled* The Art of RF System Design *on his web site:* **members.aol.com/cdrentea/myhomepage/**

Notes

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